



Features

- Wide Input Voltage from 9V to 40V
- Up to 3A Output Current
- Adjustable Output Voltage up to 20V
- High Efficiency Up to 93%
- CC/CV control
- Internal Soft-Start
- Auto Recovery after Faults
- Output Load Voltage Drop Compensation
- Programmable Over Current Setting
- Output Over-Voltage Protection
- Over-Temperature Protection
- Thermal Enhanced ESOP8 Package
- RoHS Compliant

Applications

- Car Charger
- Rechargeable Portable Device
- Automotive Industry

General Description

The TX9533 is a monolithic, CC/CV step-down switch mode converter with a built-in high-side power MOSFET. It achieves 3A continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. Fault condition protection

includes cycle-by-cycle current limiting and thermal shutdown.

The TX9533 is available in an ESOP8 package, provides a very compact system solution and good thermal conductance.

Typical Application

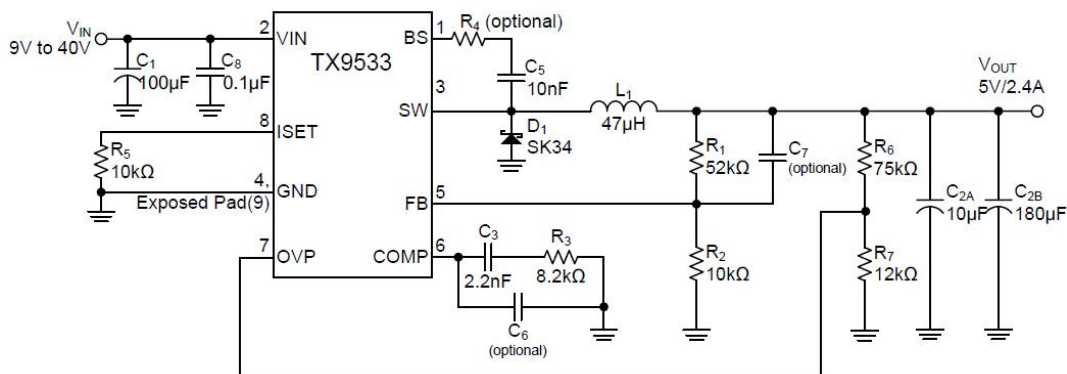


Figure 1 Typical Application Circuit

V _{OUT} (V)	R ₁ (kΩ)	R ₂ (kΩ)	R ₃ (kΩ)	C ₃ (nF)	C ₆	L ₁ (µH)	C _{2A} (µF)	C _{2B} (µF)
5	52	10	8.2	2.2	NA	47	10µF 6.3V/Ceramic	180 6.3V/30mΩ
5	52	10	8.2	2.2	NA	47	10µF 6.3V/Ceramic	470 6.3V/30mΩ

Table 1 Recommended Component Selection



System Block Diagram

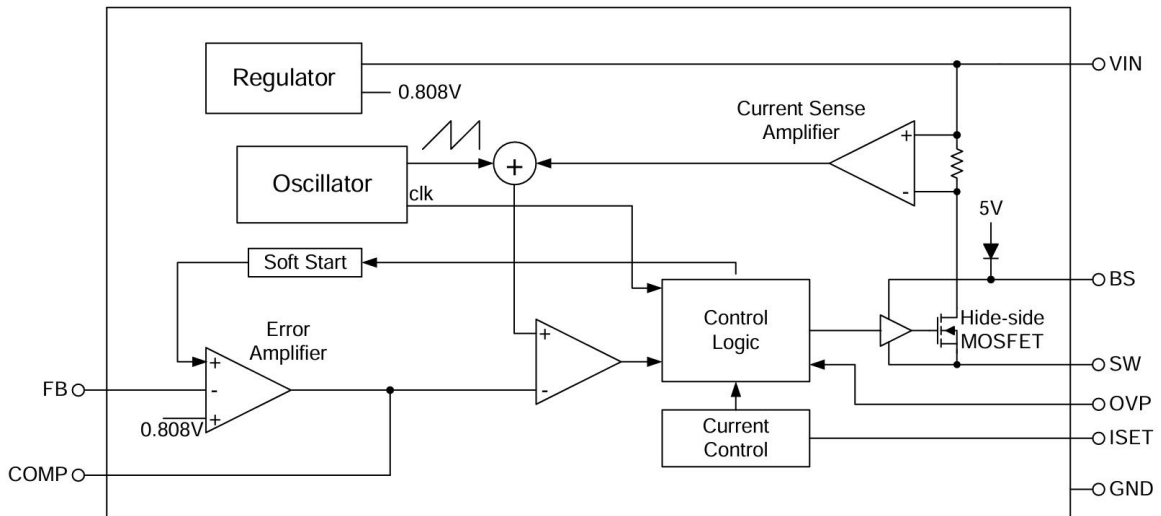


Figure 2 TX9533 Functional Block Diagram

Function Description

The TX9533 is a constant frequency current mode step-down asynchronous DC/DC converter. It regulates input voltage from 9V to 40V, down to an output voltage as low as 1V, and can provide up to 3A of continuous load current.

Control Loop

During normal operation, the output voltage is sensed at FB pin through a resistive voltage divider and amplified through the error amplifier. The voltage of error amplifier output pin – COMP is compared to the switch current to controls the RS latch. At each cycle, the high side NMOS would be turned on when the oscillator sets the RS latch and would be turned off when current comparator resets the RS latch. When the load current increases, the FB pin voltage drops below 0.808V, it causes the COMP voltage increase until average inductor current arrive at new load current.

Input Under Voltage Lockout

When the TX9533 power on, the internal circuits are held inactive until VIN exceeds the input UVLO threshold voltage. And the regulator will be disabled when VIN

below the input UVLO threshold voltage.

Over Current Protection

ISET pin is connected to a resistor to set output current limit value. At this point, the device will transition from regulating output voltage to regulating output current, and the output voltage will drop with increasing load. The oscillator normally switches at 125kHz. However, if the FB voltage drops down, then the switching frequency decreases. Once the overload condition is removed, the frequency will return to normal.

Over Temperature Protection

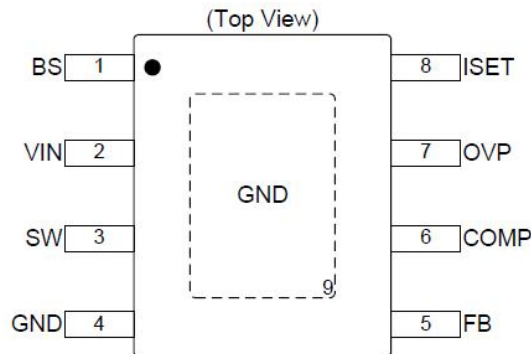
The TX9533 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown.

Compensation

The stability of the feedback circuit is controlled through COMP pin. The compensation value of the application circuit is optimized for particular requirements. If different conversions are requires, some of the components may need to be changes to ensure stability.



Pin Configuration



Pin Description

Pin NO.	Pin Name	Pin Description
1	BS	High Side Gate Drive Boost Input. A 22nF or greater capacitor must be connected from this pin to SW. It can boost the gate drive to fully turn on the internal high side NMOS.
2	VIN	Power Supply Input Pin. Drive 9V to 40V voltage to this pin to power on this chip. Connecting a bypass capacitor ($\geq 22\mu\text{F} \times 2$) between VIN and GND to eliminate noise.
3	SW	Power Switching Output. It is the output pin that internal high side NMOS switching to supply power.
4	GND	Ground Pin.
5	FB	Voltage Feedback Input Pin. Connecting FB and VOUT with a resistive voltage divider. This IC senses feedback voltage via FB and regulate it at 0.808V.
6	COMP	Compensation Pin. This pin is used to compensate the regulation control loop. Connect a series RC network from COMP pin to GND.
7	OVP	OVP Input Pin. If the voltage at this pin is over 0.8V, the IC shuts down the high-side switching MOSFET.
8	ISET	Output Current Setting Pin. Connect a resistor between ISET and GND pin to set output current.
9	GND	Exposed Pad. Connecting to Pin 4.



Order Information

Part Number	Package	Shipment
TX9533	ESOP8	Tape & Reel / 4000

Absolute Maximum Ratings ⁽¹⁾

Input Supply Voltage V_{IN}-0.3V ~ 42V
 SW Voltage V_{SW}-0.3V (-5V for < 10ns)
 ~ 42V (44V for < 5ns)
 Boost Voltage V_{BS}-0.3 ~ ($V_{SW} + 6V$)
 All Other Pins Voltage.....-0.3V ~ 6V

Maximum Junction Temperature.....150°C
 Storage Temperature.....-55°C ~ 150°C
 ESD Classification (HBM) Class 2
 Power Dissipation (PD) @ $T_A = 25^\circ C$1.333W
 Lead Temperature (Soldering 10sec)260°C

Recommended Operating Conditions ⁽²⁾

Input Supply Voltage V_{IN} 9V ~ 40V
 Junction Temperature T_J-40°C~125°C

Ambient Temperature T_A -40°C~85°C

Thermal Characteristics

ESOP8, θ_{JA}75°C/W

ESOP8, θ_{JC}15°C/W

Notes (1): Stresses exceed those ratings may damage the device.

Notes (2): If out of its operation conditions, the device is not guaranteed to function.

**Electrical Characteristics** $V_{IN}=12V$, $T_A=25^{\circ}C$, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
Quiescent Current (non-switching)	I_Q	$V_{FB} = 1V$	---	0.9	1.4	mA
Standby Supply Current (no loading)	---	$V_{OUT} = 5V$	---	3	---	mA
Reference Voltage						
Feedback Voltage	V_{FB}	$9V \leq V_{IN} \leq 40V$	792	808	824	mV
Input UVLO						
UVLO Threshold	---	V_{IN} Rising	8	8.5	8.9	V
Hysteresis	---	V_{IN} Falling	---	1.2	---	V
OVP Threshold						
OVP Threshold Voltage	V_{OVP}	V_{OVP} Rising	---	0.8	---	V
Oscillator						
Switching Frequency	f_{SW}	$V_{FB} = 0.808V$	90	125	160	kHz
Foldback Switching Frequency	---	$V_{FB} = 0V$	---	30	---	kHz
Maximum Duty Cycle	D_{MAX}	---	80	86	91	%
Minimum on time	$T_{ON(MIN)}$	$V_{FB} = 0.7V$	---	200	---	ns
MOSFET						
High Side MOSFET On Resistance ⁽³⁾	$R_{DS(on)h}$	At $25^{\circ}C$	---	95	---	m Ω
Current Limit						
Current Limit	I_{LIM}	---	---	4.5	---	A
Error Amplifier						
Error Amplifier Transconductance ⁽³⁾	G_{EA}	$\Delta I_{COMP} = \pm 10\mu A$	---	650	---	$\mu A/V$
Error Amplifier Voltage Gain ⁽³⁾	A_{EA}	---	---	4000	---	V/V
Current Sense Transconductance ⁽³⁾	G_{CS}	---	---	5.25	---	A/V
Current Setting						
ISET Voltage	---	---	---	1	---	V
ISET to IOUT Current Gain ⁽³⁾	---	I_{OUT}/I_{SET} , $R_{ISET}=19.6k\Omega$	---	25000	---	A/A
Current Controller DC Accuracy ⁽³⁾	---	$R_{ISET}=19.6k\Omega$ $V_{OUT}=3.5V$ Open-Loop DC Test	---	1190	---	mA
Thermal Shutdown						
Thermal Shutdown threshold ⁽³⁾	---	---	---	160	---	$^{\circ}C$

Note:(3) Guaranteed by design.

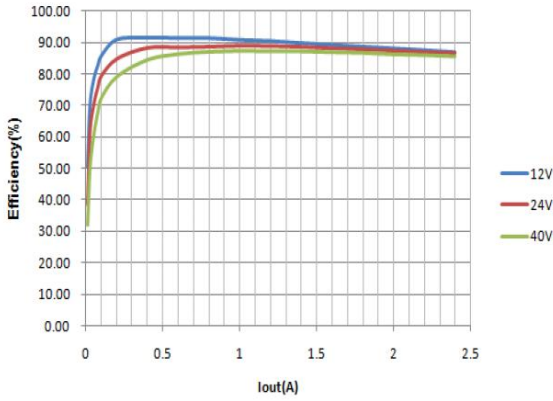


Typical Performance Characteristics

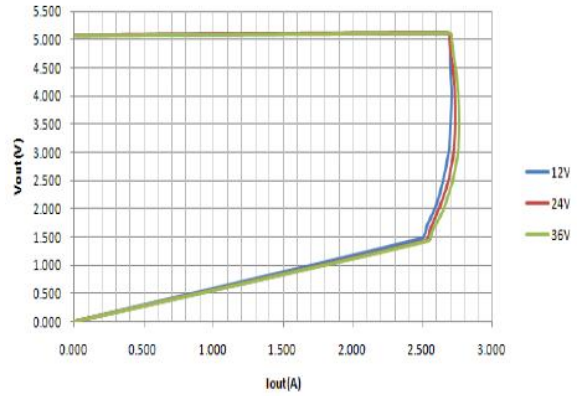
C1 = 100uF , C2 = 10uF+180uF, L1 = 47uH,R5=10K , TA = +25°C, unless otherwise noted.

Efficiency Test

Vout=5V

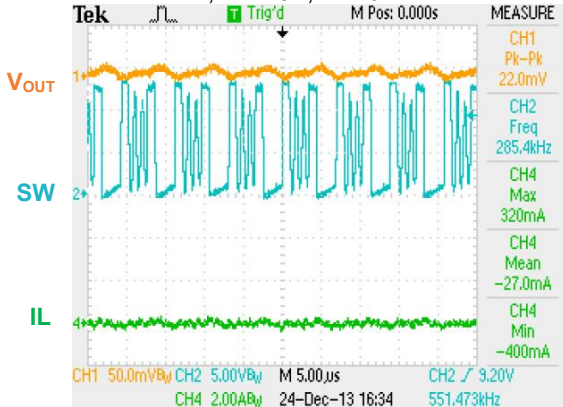


CC/CV Curve



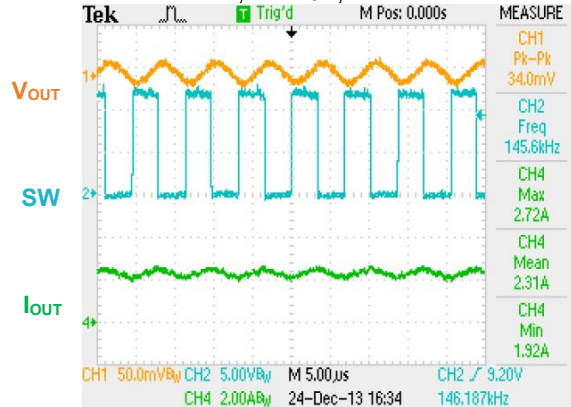
Steady State

Vin=12V, Vout=5V, Iout=0A



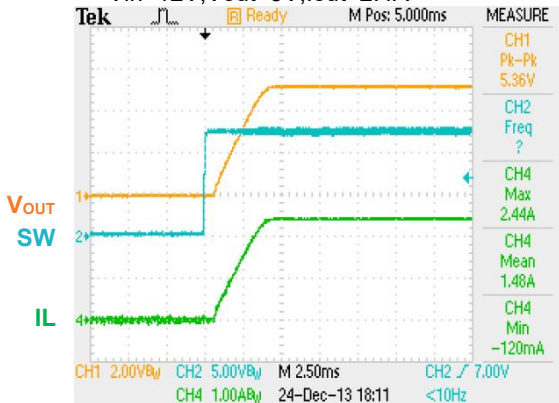
Steady State

Vin=12V, Vout=5V, Iout=2.4A



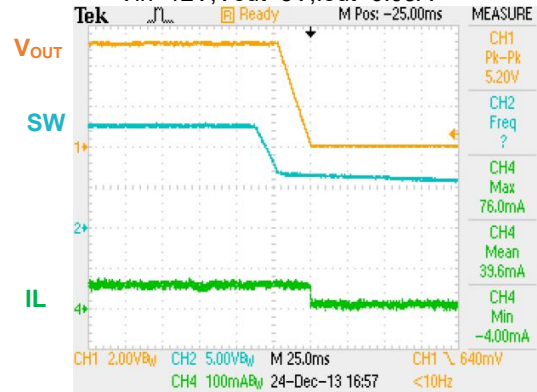
Power On

Vin=12V, Vout=5V, Iout=2.4A



Shut Down

Vin=12V, Vout=5V, Iout=0.05A





Applications Information

Output Voltage Setting

The output voltage VOUT is set using a resistive divider from the output to FB. The FB pin regulated voltage is 0.808V. Thus the output voltage is:

$$V_{out} = 0.808 * (1 + R1/R2) V$$

Table2 lists recommended values of R1 and R2 for most used output voltage:

Table2 Recommended Resistance Values

Place resistors R1 and R2 close to FB pin to prevent stray

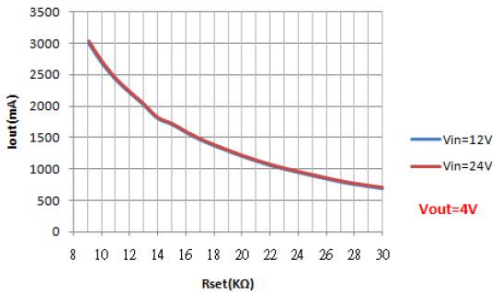
VOUT	R1	R2
5V	52K	10K
3.3V	30.9K	10K

pickup.

Current Limit Setting

TX9533 current limit value is set by a resistor connected between the ISET pin and GND. The output current is linearly proportional to the current flowing out of the ISET pin. The voltage at ISET is roughly 1V and the current gain from ISET to output is roughly 25000 (25mA/1µA).

To determine the proper resistor for a desired current, please refer to below:



Current Limit Line Compensation

When operating at current limit mode, the current limit increase slightly with input voltage. For wide input voltage application, a resistor RC is added to compensate line change and keep output high current limit accuracy, as shown in Figure 3.

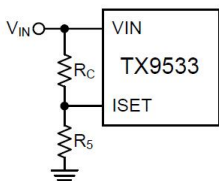


Figure 3 Input Line Compensation

Input Capacitor Selection

The use of the input capacitor is controlling the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 times to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IN(RMS)} = I_{OUT} * \sqrt{D * (1 - D)}$$

Where D is the duty cycle and the value is VOUT / VIN. A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When tantalum or electrolytic capacitors is used, a 0.1µF ceramic capacitor should be placed as close to the IC as possible.

Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. Low ESR capacitors are preferred. Ceramic, tantalum or low ESR electrolytic capacitors can be used, depends on the output ripple requirement. Add a 100µF or 470µF low ESR electrolytic capacitor when operated in high input voltage range (VIN > 20V). It can improve the device's stability. The output ripple voltage ΔVOUT is described as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s * L} * (1 - \frac{V_{OUT}}{V_{IN}}) * (RESR + \frac{1}{8 * f_s * C_2})$$

Where fs is the switching frequency, L is the inductance value, VIN is the input voltage, VOUT is the output voltage, RESR is the equivalent series resistance value of the output capacitor, and the C2 is the output capacitor. When using the ceramic capacitors, the RESR can be ignored and the output ripple voltage ΔVOUT is shown as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 * f_s^2 * L * C_2} * (1 - \frac{V_{OUT}}{V_{IN}})$$

When using tantalum or electrolytic capacitors, typically 90% of the output voltage ripple is contributed by the ESR of output capacitors. the output ripple voltage ΔVOUT can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s * L} * (1 - \frac{V_{OUT}}{V_{IN}}) * RESR$$

The characteristics of the output capacitor also affect the stability of the regulation system. The TX9533 can be optimized for a wide range of capacitance and ESR values



Inductor

The output inductor is used for store energy and filter output ripple current. A large value inductor will result in less ripple current and lower output ripple voltage. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode. That will lower ripple current and results in lower output ripple voltage. A good rule for determining the inductance is set the peak-to-peak inductor ripple current ΔI almost equal to 30% of the maximum load current. Then the minimum inductance can be calculated with the following equation:

$$L \geq \frac{V_{OUT}}{f_s \cdot \Delta I} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$\Delta I = 0.3 * I_{LOAD(MAX)}$$

Where V_{IN} is the input voltage, f_s is the switching frequency, ΔI is the peak-to-peak inductor ripple current and $I_{LOAD(MAX)}$ is the maximum load current.

Choose an inductor that will cause the peak inductor current satisfying the equation:

$$I_{LP} = I_{LOAD(MAX)} + \frac{V_{OUT}}{2 * f_s * L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \leq LIMIT$$

Where I_{LIMIT} is the high-side MOSFET current limit value.

Rectifier Diode

During the transition between switching MOSFETs, a Schottky diode should be connected between SW pin and GND pin. The Schottky diode must have current rating higher than the maximum

Compensation Components

The system stability and transient response are controlled through the COMP pin. Selecting the appropriate compensation value by the following procedure:

1. Calculate the R_3 value with the following equation:

$$R_3 < \frac{2\pi * C_2 * f_s * V_{OUT}}{10 * G_{EA} * G_{CS} * V_{FB}}$$

where G_{EA} is the error amplifier transconductance, and G_{CS} is the current sense transconductance.

2. Calculate the C_3 value with the following equation:

$$C_3 > \frac{4 * 10}{2\pi * R_3 * f_s}$$

3. If the C_2 ESR zero is less than half of the switching frequency, use C_6 to cancel the ESR zero:

$$C_6 = \frac{C_2 * RESR}{R_3}$$

External Boost Diode Selection

For duty cycle larger than 65% applications, it is recommended that an external boost diode be added. This helps improve the efficiency. The boost diode can be a low cost one such as 1N4148.

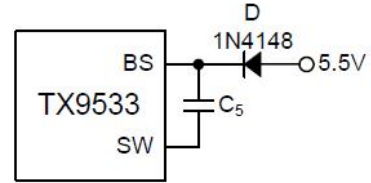


Figure 4 External Boost Diode

PCB Layout Recommendation:

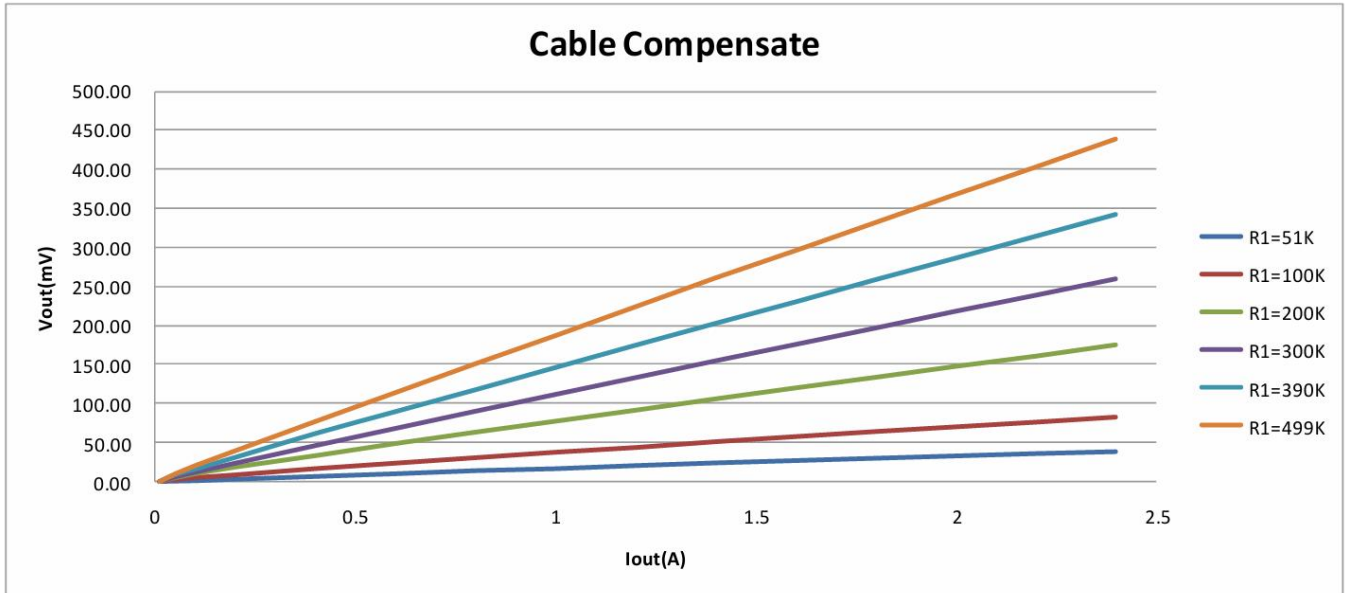
The device's performance and stability is dramatically affected by PCB layout. It is recommended to follow these general guidelines show below:

1. Keep the traces of the main current paths as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{IN} bypass capacitor (C_{IN}) close to the device pins (V_{IN} and GND). The loop area formed by C_{IN} and V_{IN}/GND pins must be minimized.
3. Place feedback resistors close to the FB pin. Connect feedback network behind the output capacitors.
4. Place compensation components close to the COMP pin.
5. Keep the sensitive signal (FB, COMP, ISET) away from the switching signal (SW).
6. Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacities.
7. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connects to the exposed pad should be maximized to improve thermal performance.
8. Multi-layer PCB design is recommend.



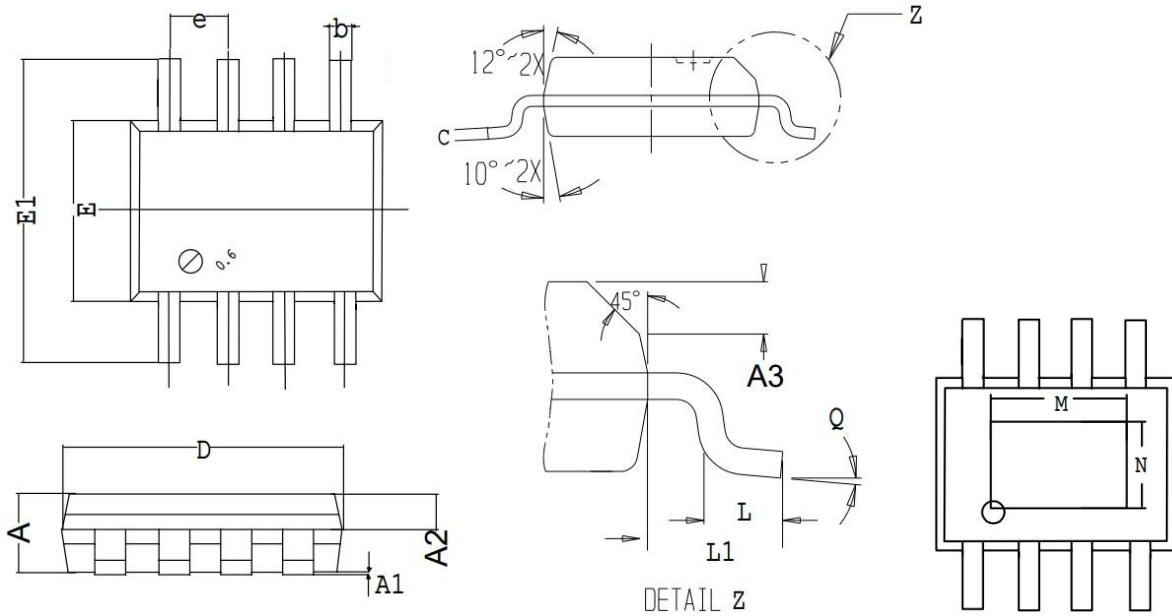
Stability Compensation

R1 is the high side resistor of voltage divider. In the case of high R1 used, the frequency compensation needs to be adjusted correspondingly. As show in Figure 1, adding a capacitor(C7) in paralalled with R1 or increasing the compensation capacitance(C3、C6) at COMP pin helps the system stability.





ESOP8 PACKAGE INFORMATION



COMMON DIMENSIONS			
UNITS MEASURE=MILLIMETER			
SYMBOL	MIN	MID	MAX
A	1.35	1.45	1.55
A1	0.00	0.05	0.10
A2	0.65	0.70	0.75
A3	0.35	0.40	0.45
b	0.35	0.40	0.45
c	0.18	0.20	0.22
D	4.70	4.90	5.10
e	-	1.27TYP	-
E1	5.80	6.10	6.20
E	3.80	3.90	4.00
L	0.40	0.60	0.80
Q	0°	/	8°
M	3.10	3.20	3.30
N	2.20	2.30	2.40
L1	1.05REF		



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