Features

- Wide Input Voltage from 4.75V to 40V
- Up to 3.5A Output Current
- USB-PD Type-C Support
- Adjustable Output Voltage from 3.3V up to 20V
- High Efficiency Up to 93%
- High Duty-Cycle Up to 96%
- Internal Soft-Start
- Thermal Enhanced TSSOP-14, QFN4*4-16L Package
- Auto Recovery into Full Load after Faults
- Low Output Short Current
- Output Cord Voltage Drop Compensation
- Programmable Over Current Setting
- Input Over-Voltage Protection
- Over-Temperature Protection
- ROHS Compliant

Applications

- Car Charger
- Rechargeable Portable Device
- CC/CV regulation converter

General Description

The TX9565 is a CC/CV step-down switch mode converter with a built-in high-side power MOSFET and a gate driver for a low side external power MOSFET It achieves 3.5A continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. The converter can be configured as single output or dual outputs with independent over current protection (OCP). Fault condition protections include cycle-by-cycle current limit and thermal shutdown.

The TX9565 is available in a TSSOP-14,QFN4*4-16L packages, provides a very compact system solution and good thermal conductance.

Typical Application

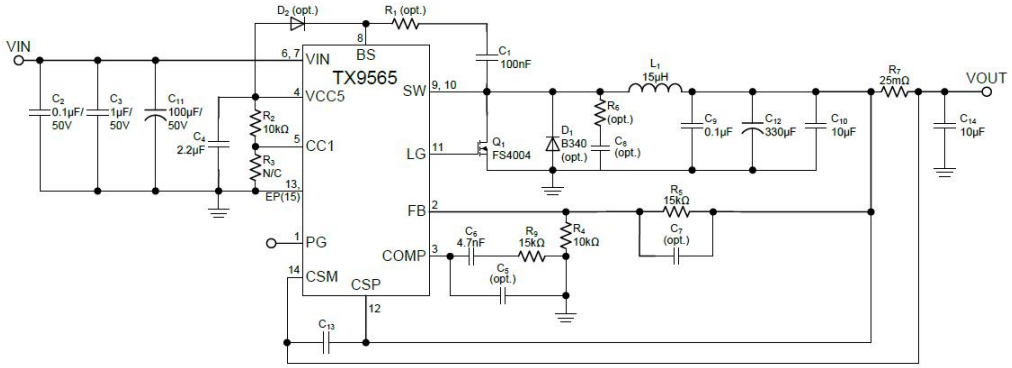


Figure 1 Simplified Application Circuit

System Block Diagram

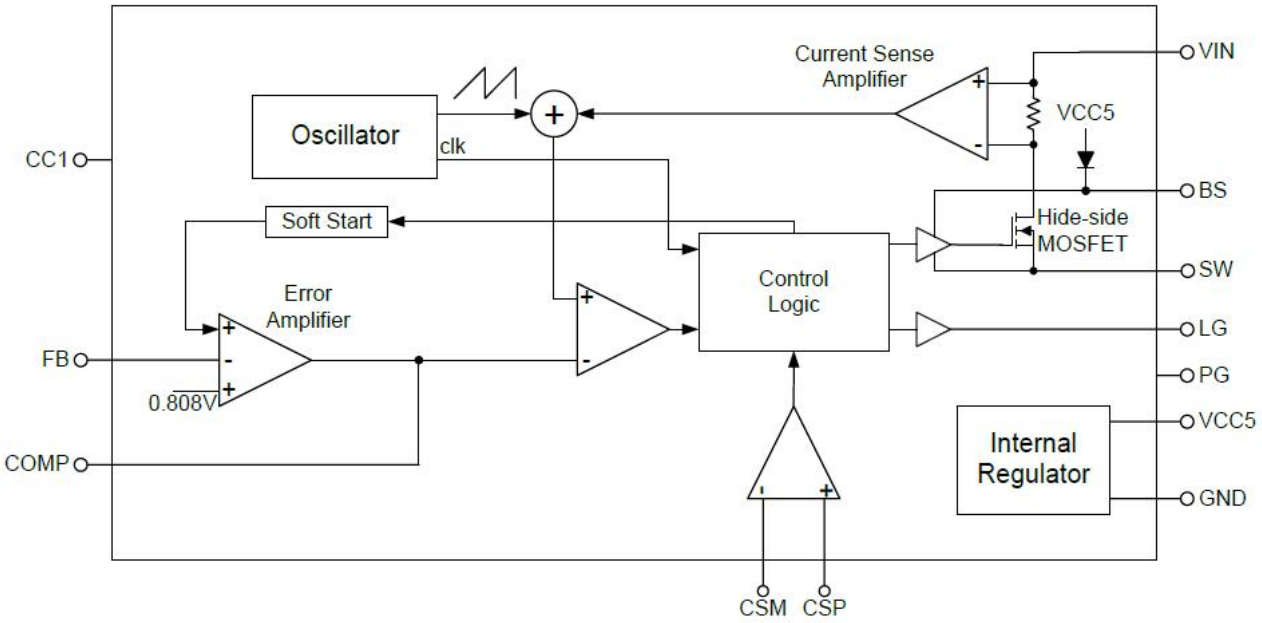
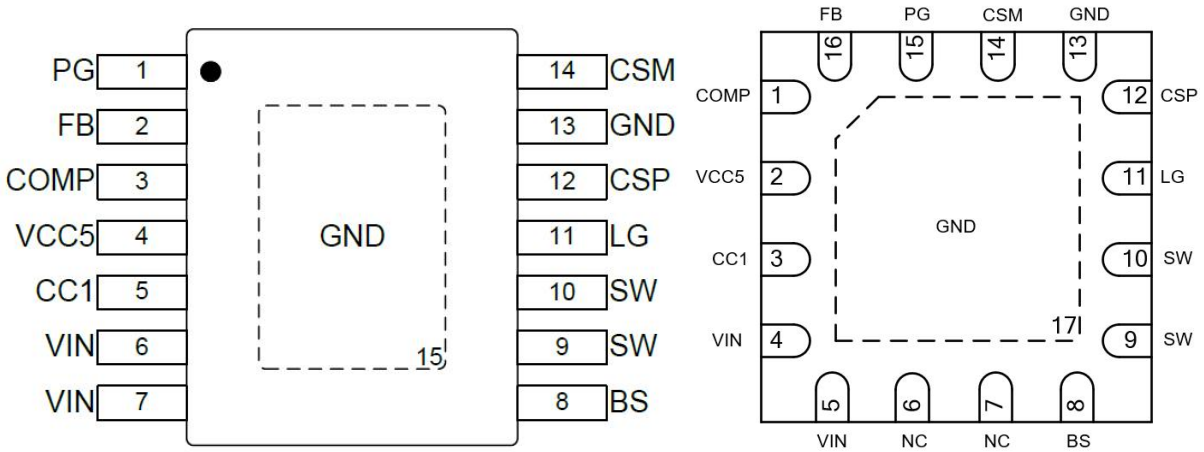


Figure 2 TX9565 Functional Block Diagram

Pin Configuration



Pin Function Description

Pin NO.		Pin Name	Pin Description
TSSOP14L	QFN4×4-16L		
1	15	PG	Power good Pin.
2	16	FB	Voltage Feedback Input Pin Connecting FB and VOUT with a resistive voltage divider. This IC senses feedback voltage via FB and regulate it at 0.808V.
3	1	COMP	Compensation Pin. This pin is used to compensate the regulation control loop. Connect a series RC network from COMP pin to GND.
4	2	VCC5	LG Driver Bias Supply Decouple with a 2.2uF capacitor.
5	3	CC1	Connect to VCC5 with a 10kΩresistor for 5V USB Type-C application.
6,7	4,5	VIN	Power Supply Input Pin. Drive 4.75V to 40V voltage to this pin to power on this chip Connecting a 10uF ceramic bypass capacitor between VIN and GND to eliminate noise.
8	8	BS	High Side Gate Drive Boost Input. A 22nF or greater capacitor must be connected from this pin to SW. It can boost the gate drive to fully turn on the internal high side NMOS.
9,10	9,10	SW	Power Switching Output. It is the output pin that internal high side NMOS switching to supply power.
11	11	LG	Gate Driver Output. Connect this pin to the gate of the external low-side Power MOSFET.
12	12	CSP	Positive input pin for output load current sensing.
13	13	GND	Ground Pin.
14	14	CSM	Negative input pin for output load current sensing.
15	17	GND	Exposed Pad Connecting to Pin 13.

Order Information

Part Number	Package	Shipment
TX9565TP14R	TSSOP14	Tape & Reel / 4000
TX9565FTR	QFN4*4-16L	Tape & Reel / 3000

Absolute Maximum Ratings(1)

Input Supply Voltage V_{IN}……..-0.3V ~ 42V

SW Voltage V_{SW}…….....-0.3V(-5V for < 10ns) ~ 42V (46V for < 5ns)

Boost Voltage V_{BS}……..……-0.3 ~ (V_{SW} +6V)

All Other Pins Voltage……..-0.3V ~ 6V

Maximum Junction Temperature……....150°C

Storage Temperature……..... -55°C ~ 150°C

Lead Temperature (Soldering 10sec)……..... 260°C

ESD Classification(HBM)…….....Class 2

Power Dissipation (P_D)TSSOP-14 @T_A = 25°C 2.5W

Power Dissipation (P_D)QFN4*4-16@T_A = 25°C ... 2.63W

Recommended Operating Conditions(2)

Input Supply Voltage VIN……9V ~ 40V

Ambient Temperature TA…….....-40°C~125°C

Thermal Characteristics

TSSOP14, θJA……40°C/W

QFN4*4-16, θJA ……...……...…..38°C/W

Notes(1):Stresses exceed those ratings may damage the device.

Notes(2):If out of its operation conditions, the device is not guaranteed to function.

Electrical Characteristics

V_{IN}=12V, T_A=25℃, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN} Input Supply Voltage	---	---	4.75	---	40	V
Quiescent Current (non-switching)	I_Q	V_{FB}=1V	---	1.5	2	mA
Standby Supply Current (no loading)	---	---	---	6	---	mA
Feedback Voltage	V_{FB}	9V≦V_{IN}≦40V	792	808	824	mV
High-Side MOSFET-On Resistance(3)	$R_{DS(ON)}$	At 25°C	---	70	---	mΩ
High-Side MOSFET Leakage Current	---	V_{EN}= 0V, V_{SW}= 0V	---	---	10	uA
High-Side MOSFET Current Limit(3)	---	Duty=65%	---	4.5	---	A
COMP to Current sense Transconductance	G_{CS}	---	---	4.6	---	A/V
Error Amplifier Transconductance	G_{EA}	∆ I_{COMP}=±10μA	---	650	---	μA/V
Error Amplifier Voltage Gain	A_{EA}	---	---	4000	---	V/V
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V	95	96	98	%
Minimum On Time	T_{ON}	---	---	250	---	ns
Oscillation frequency	F_{OSC}	---	160	220	280	KHz
Input UVLO Threshold	---	V_{IN} Rising	---	4.2	4.5	V
Input UVLO Threshold Hysteresis	---	---	---	650	---	mV
Input Over Voltage Lockout Threshold	---	V_{IN} Rising	---	38	---	V
Input OVLO Threshold Hysteresis	---	---	---	3.5	---	V
Soft-Start Start Period	---	---	---	3	---	mS
Cord Compensation(3)	---	V_{IN}=12V,R_5=51K,I_{OUT}=1A	---	26	---	mV
Thermal Shutdown Threshold(3)	---	---	---	160	---	℃
LG Driver Bias Supply Voltage	V_{CC5}	---	4.5	5	---	V
Gate Driver Sink Impedance(3)	R_{Sink}	---	---	0.9	---	Ω
Gate Driver Source Impedance(3)	R_{Source}	---	----	3.3	---	Ω
Current sense reference voltage(3)	∆ V_{CS}	V_{CSP}–V_{CSM}(R_7=20mΩ)	---	60	---	mV

Notes(3):Guaranteed by design.

Applications Information

Output Voltage Setting

The output voltage V_{OUT} is set using a resistive divider from the output to FB. The FB pin regulated voltage is 0.808V. Thus the output voltage is:

$$V_{OUT} = 0.808\times (1+\frac{R_5}{R_4})V$$

Place resistors $R_1$and R_2close to FB pin to prevent stray pickup.

Input Capacitor Selection

The use of the input capacitor is controlling the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 times to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IIN(RMS)}= I_{OUT} X \sqrt{D * (1 - D)}$$

Where D is the duty cycle and the value is VOUT/ VIN. A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice When using tantalum or electrolytic capacitors, a 0.1uF ceramic capacitor should be placed as close to the IC as possible.

Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. Low ESR capacitors are preferred Ceramic, tantalum or low ESR electrolytic capacitors can be used, depends on the output ripple requirement. Add a 100uF or 470uF low ESR electrolytic capacitor when operated in high input voltage range (V_{IN} > 20V). It can improve the device's stability. The output ripple voltage ΔV_{OUT} is described as:

$$\Delta V_{OUT}=\frac{V_{OUT}}{fs.L} * (1 - \frac{V_{OUT}}{V_{IN}})(R_{ESR}+\frac{1}{8*fs*C_{OUT}})$$

Where f_S is the switching frequency, L is the inductance value, V_{IN} is the input voltage, V_{OUT} is the output voltage, R_{ESR} is the equivalent series resistance value of the output capacitor, and the C_{OUT} is the output capacitor. When using the ceramic capacitors, the R_{ESR} can be ignored and the output ripple voltage ΔV_{OUT} is shown as:

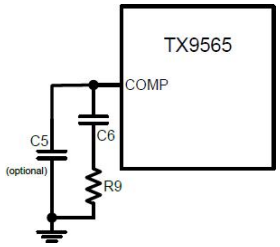
$$\Delta V_{OUT}=\frac{V_{OUT}}{8*fs^2*L*C_{OUT}}*(1-\frac{V_{OUT}}{V_{IN}})$$

When using tantalum or electrolytic capacitors, typically 90% of the output voltage ripple is contributed by the ESR of output capacitors. the output ripple voltage ΔV_{OUT} can be estimated as:

$$\Delta V_{OUT}=\frac{V_{OUT}}{fs*L} * (1 - \frac{V_{OUT}}{V_{IN}})*R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. TX9565 can be optimized for a wide range of capacitance and ESR values.

Compensation Components Selection



Selecting the appropriate compensation value by following procedures:

1. Calculate the R9value with the following equation:

$$R9=\frac{2\Pi*C_{OUT}*0.1*F_{OSC}*V_{OUT}}{G_{EA}*G_{CS}*V_{REF}}$$

where GEA is the error amplifier voltage gain and GCS is the current sense gain.

2. Calculate the C6value with the following equation:

$$C6=\frac{4}{2\Pi*R9*0.1*F_{OSC}}$$

3. If the COUT ESR zero is less than half of the switching frequency, use C5to cancel the ESR zero:

$$C5=\frac{C_{OUT}*R_{ESR}}{R9}$$

Output Current Setting

The output current IOUT can be estimated as:

$$I_{OUT}(A)=\frac{60(mv)}{R_7(m\Omega)}$$

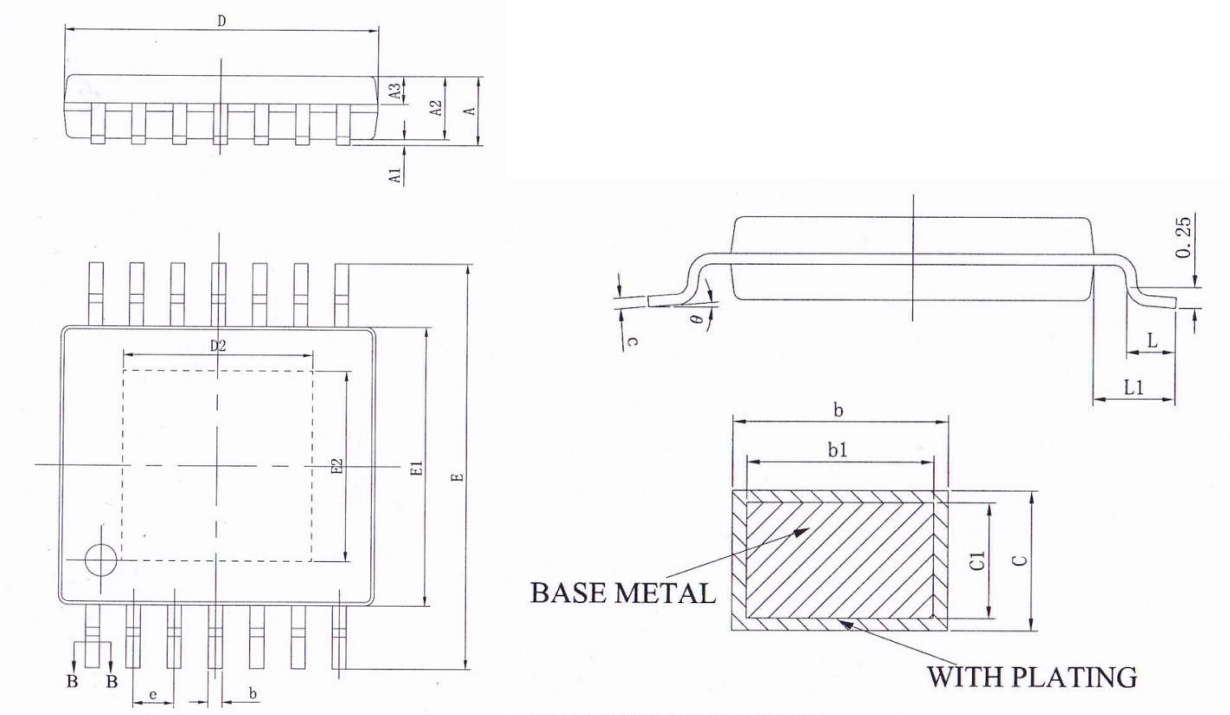
R7 is the output current sensing resistance.

PCB Layout Guideline

The device's performance and stability is dramatically affected by PCB layout. It is recommended to follow these general guidelines show bellow:

1. Keep the traces of the main current paths as short and wide as possible to minimize parasitic inductance and resistance.
2. Place VIN bypass capacitor (CIN)close to the device pins (VIN and GND) The loop area formed by CIN and VIN/GND pins must be minimized.
3. Minimize the switching loop area formed by SW and the power MOSFET of LG.
4. Use a combination of bulk capacitors and smaller ceramic capacitors with low series impedance for the input and output capacitors. Place the smaller capacitors closer to the IC.
5. Place feedback resistors close to the FB pin. Connect feedback network behind the output capacitors.
6. Place compensation components close to the COMP pin.
7. Place the BS bootstrap capacitor close to the IC and connect directly to the BS to SW pins.
8. Keep the sensitive signal (FB, COMP, CSP, CSM, CC1) away from the switching signal (SW, LG).
9. Use Kelvin connections to sense resistor for the current sense signals CSP and CSM.
10. Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacities.
11. Place the VCC5 bypass capacitor close to the controller IC, between the VCC5 and GND pins.
12. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connects to the exposed pad should be maximized to improve thermal performance.
13. Multi-layer PCB design is recommended.

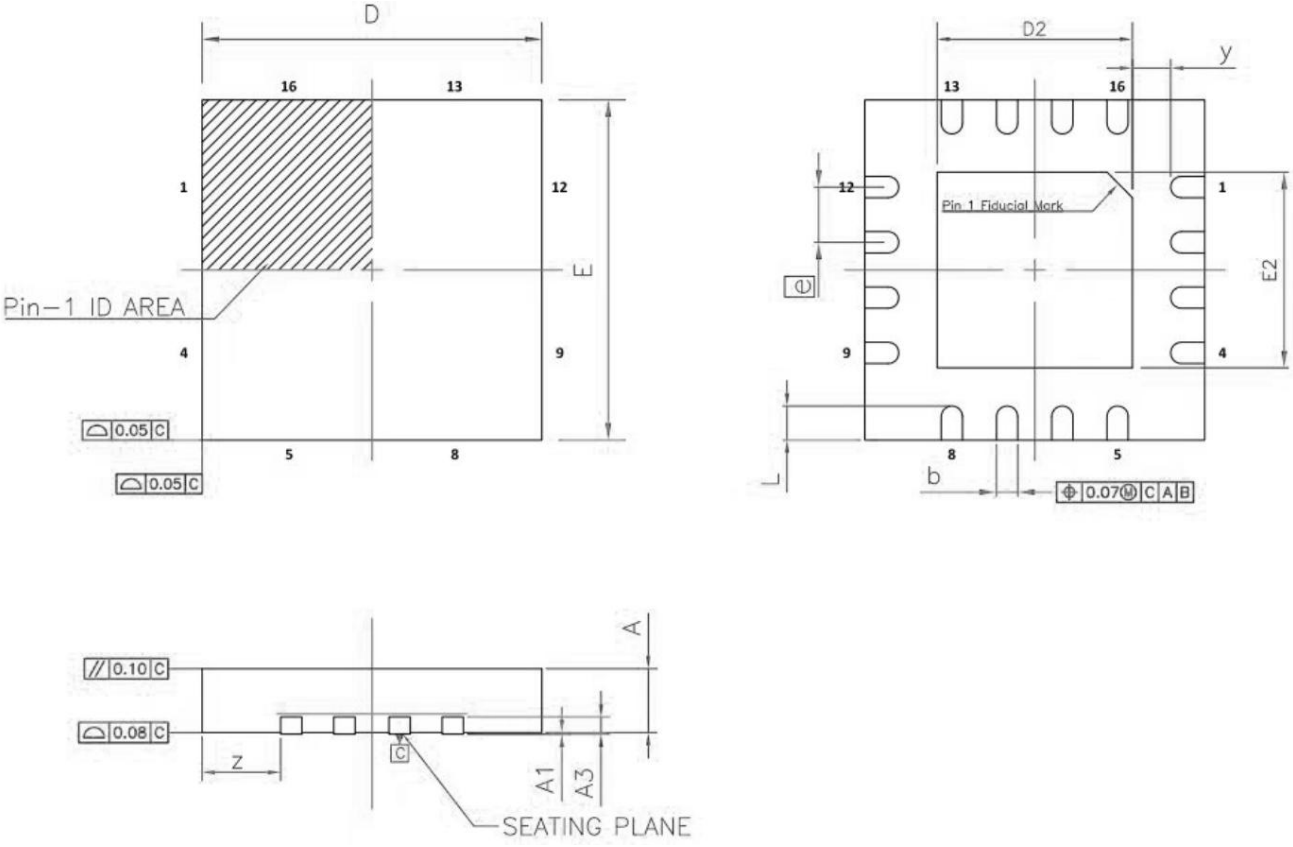
TSSOP14 PACKAGE INFORMATION



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

Size (mm) / L/F Size (mil)	D2	E2
79*79	1.80REF	1.80REF
124*122	2.95REF	2.90REF

QFN4*4-16L PACKAGE INFORMATION



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.95	4.00	4.05
E	3.95	4.00	4.05
D2	2.20	2.30	2.40
E2	2.20	2.30	2.40
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
e	0.650 BSC		
K	---	---	---
L	0.35	0.40	0.45
Y	0.450 REF		
Z	0.925 REF		