Features

- Single Inductor Buck-Boost Controller for Step-Up/Step-Down DC/DC Conversion
- Wide Input Voltage from 4.5V to 40V
- High Efficiency
- Adjustable Switching Frequency
- Programmable External Soft-Start
- Auto Recovery after Faults
- Output Cord Voltage Drop Compensation
- Programmable Over Current Setting
- Power Good and Output Overvoltage Protection
- Over-Temperature Protection
- Thermal Enhanced QFN4x4-24L Package
- RoHS Compliant

Applications

- Car Charger
- Rechargeable Portable Devices
- USB Power Delivery
- Automotive Industry

General Description

The TX9575 is a synchronous four-switch buck-boost DC/DC controller capable of regulating the output voltage at, above, or below the input voltage. The TX9575 operates over a wide input voltage range of 4.5 V to 40 V to support a variety of applications.

The TX9575 employs current-mode control both in buck and boost modes of operation for superior load and line regulation. The switching frequency is programmed by an external resistor. This device also features a programmable soft-start function and offers protection features including cycle-by-cycle current limiting, input undervoltage lockout(UVLO), output overvoltage protection (OVP), and thermal shutdown.

The TX9575 is available in an QFN4x4-24L package, and provides a very compact system solution and good thermal conductance.

Typical Application

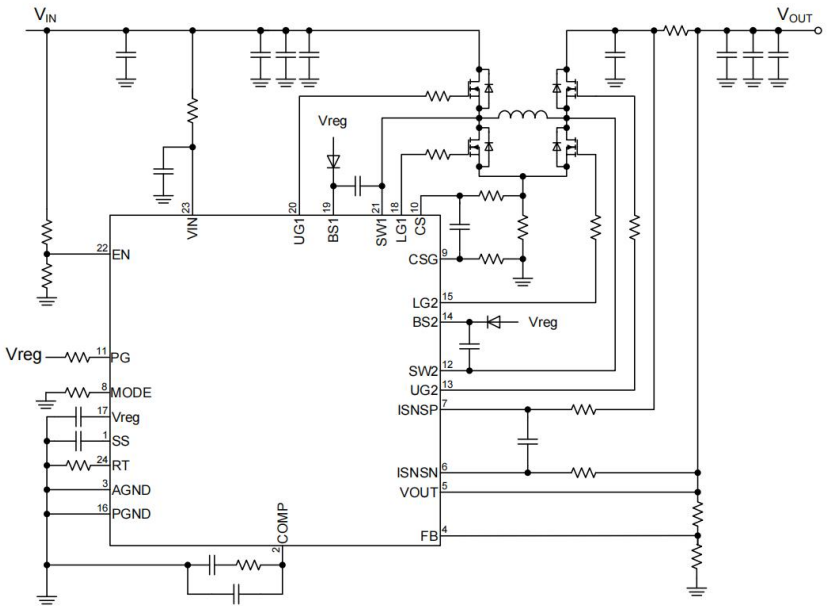
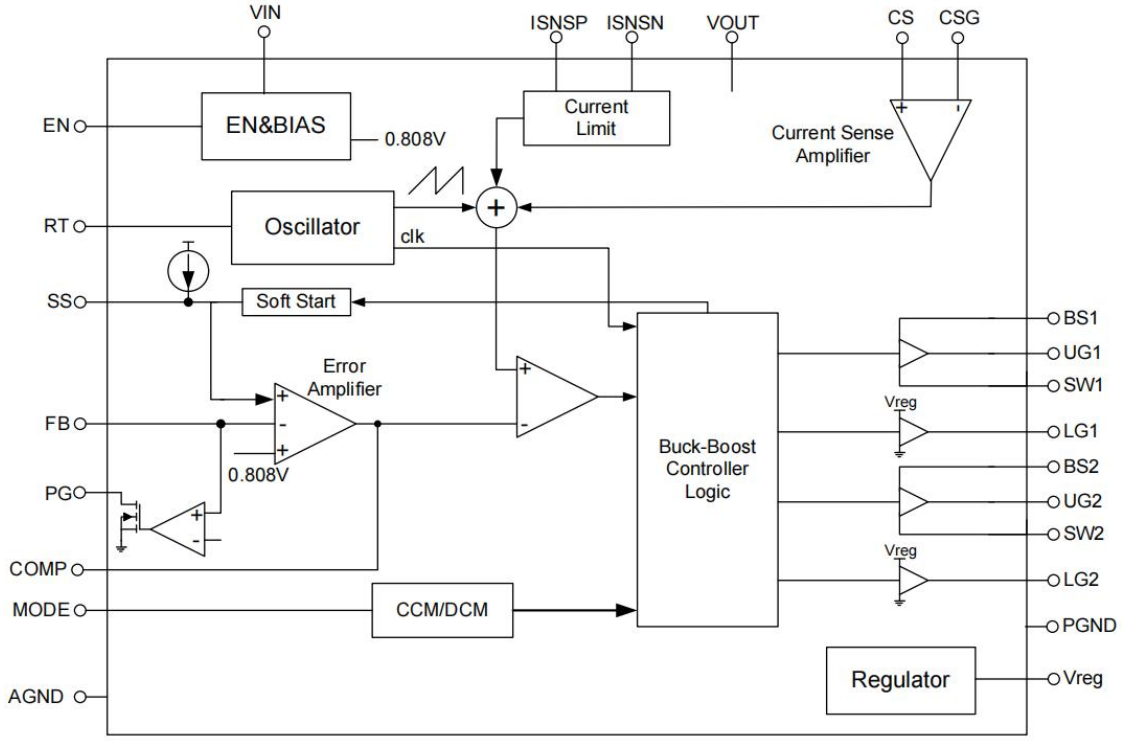


Figure 1. Typical Application Circuit

System Block Diagram



Functional Description

The TX9575 is four-switch buck-boost controller IC with integrated drivers for N-channel MOSFETs. TX9575 operates in the buck mode when VIN is greater than VOUT, in the boost mode when VIN is less than VOUT, and in the buck-boost mode when VIN is close to VOUT.

The TX9575 integrates four N-Channel MOSFET drivers including two low-side drivers and two high-side drivers, eliminating the need for external drivers or floating bias supplies. The internal VCC regulator supplies internal bias rails as well as the MOSFET gate drivers.

The PWM control scheme is based on valley current mode control for buck operation and peak current mode control for boost operation. The inductor current is sensed through a single sense resistor to ground in series with the low side MOSFETs. The sensed current is also monitored for cycle-by-cycle current limit.

In addition to the cycle-by-cycle current limiting, the TX9575 also provides output current regulation that can be configured for output current limiting and short circuit protection. This is useful for battery charging or other applications where a constant current behavior may be required.

The soft-start time of TX9575 is programmed by a capacitor connected to the SS pin to minimize the inrush current and overshoot during startup. The EN/UVLO pin supports programmable input under voltage lockout (UVLO) with hysteresis. The PG output indicates when the FB voltage is inside a ±10% regulation window centered at VREF.

Control Loop

The TX9575 is a fixed frequency current modecontroller of both the buck and boost switches. During normal operation, the output voltage is sensed at FB pin through a resistive voltage divider and amplified through the error amplifier. The error amplifier produces an error voltage by driving the COMP pin. An slope compensation signal based on VIN, VOUT,is added to the current sense signal measured across the CS and CSG pins. The result is

compared to the COMP error voltage by the PWM comparator.

The TX9575 regulates the output using valley current mode control in buck mode and peak current mode control in boost mode. For valley current mode control, the high-side buck MOSFET controlled by UG1 is turned on by the PWM comparator at the valley of the inductor ripple current and turned off by the oscillator clock signal. Valley current mode control is advantageous for buck converters where the PWM controller must resolve short on-time. For peak current mode control in the boost mode, the low-side boost MOSFET controlled by LG2 is turned on by the clock signal in each switching cycle and turned off by the PWM comparator at the peak of the inductor ripple current.

The LG1 and UG1 drive signal, controls the synchronous buck stage. The LG2 and UG2 drive signal, controls the synchronous boost stage. For operation with VIN close to VOUT, the TX9575 uses a buck-boost transition scheme.

VCC Regulator

In TX9575, the VCC regulator provides a regulated 5.4V supply with adequate VIN voltage to the gate drivers. For low VIN operation, ensure that the VCC voltage is sufficient to fully enhance the MOSFETs. A 2.2-μF to 4.7uF capacitor to PGND is recommended to supply the VCC regulator load transients.

Soft Start

The TX9575 soft-start time is programmed using a soft-start capacitor from the SS pin to AGND. When the converter is enabled, an internal 6-μA current source charges the soft-start capacitor. When the SS pin voltage is below the 0.808V feedback reference voltage VREF, the soft-start pin controls the regulated FB voltage. Once SS exceeds VREF, the soft-start interval is complete and the error amplifier is referenced to VREF. The soft-start time is roughly given by below equation:

$$t_{ss} = \frac{Css \times 0.808}{6uA}$$

The soft-start capacitor is internally discharged when the converter is disabled because of EN/UVLO falling below the operation threshold or VCC falling below the VCC UV threshold. The soft-start pin is also discharged when the converter is in hiccup mode current limiting or in thermal shutdown.

Over Current Protection

The TX9575 provides cycle-by-cycle current limit to protect against overcurrent and short circuit conditions. In buck operation, the sensed valley voltage across the CSG and CS pins is limited to 76mV. The high-side buck switch skips a cycle if the sensed voltage does not fall below this threshold during the buck switch off time. In boost operation, the maximum peak voltage across CS and CSG is limited to 170mV. If the peak current in the low-side boost switch causes the CS pin to exceed this threshold voltage, the boost switch is turned off for the remainder of the clock cycle.

Output Current Limit

The TX9575 provides output current limiting capability and output short circuit protection to limit the output current of the DC/DC converter. A current sense amplifier with inputs at the ISNSP and ISNSN pins monitors the voltage across the sense resistor and compares it with an internal 50 mV reference. The current limiting feature can be used in applications requiring a regulated current from the load. The target constant current is given by below equation:

$$I_{out,AVG} = \frac{50mV}{Rsns}$$

The current loop can be disabled by shorting the ISNSP and ISNSN pins together.

Input Under Voltage Lockout

When the TX9575 power on, the internal circuits are held inactive until VIN exceeds the input UVLO threshold voltage. And the regulator will be disabled when VIN below the input UVLO threshold voltage.

Over Temperature Protection

The TX9575 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown.

Layout Guideline

The basic PCB board layout requires separation of sensitive signal and power paths. It is recommended to follow these general guidelines show bellow:

1.Keep the traces of the main current paths as short and wide as possible to minimize parasitic inductance and resistance.

2.Place the power components including the input filter capacitor CIN, the power MOSFETs of UG1 and LG1, and the sense resistor close together to minimize the loop area for input switching current in buck operation.

3.Place the power components including the output filter capacitor COUT, the power MOSFETs of UG2 and LG2, and the sense resistor close together to minimize the loop area for output switching current in boost operation.

4.Use a combination of bulk capacitors and smaller ceramic capacitors with low series impedance for the input and output capacitors. Place the smaller capacitors closer to the IC.

5.Minimize the SW1 and SW2 loop areas.

6.Place the BST1 bootstrap capacitor close to the IC and connect directly to the BST1 to SW1 pins.

7.Place the BST2 bootstrap capacitor close to the IC and connect directly to the BST2 to SW2 pins.

8.Place feedback resistors close to the FB pin. Connect feedback network behind the output capacitors.

9.Place compensation components close to the COMP pin.

10.Keep the sensitive signal (FB, COMP, ISNSP, ISNSN, CS, CSG, Vreg, VOUT, RT, SS) away from the switching signal.

11.Use Kelvin connections to sense resistor for the current sense signals CS and CSG.

12.Use Kelvin connections to sense resistor for the current sense signals ISNSP and ISNSN.

13.Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacities.

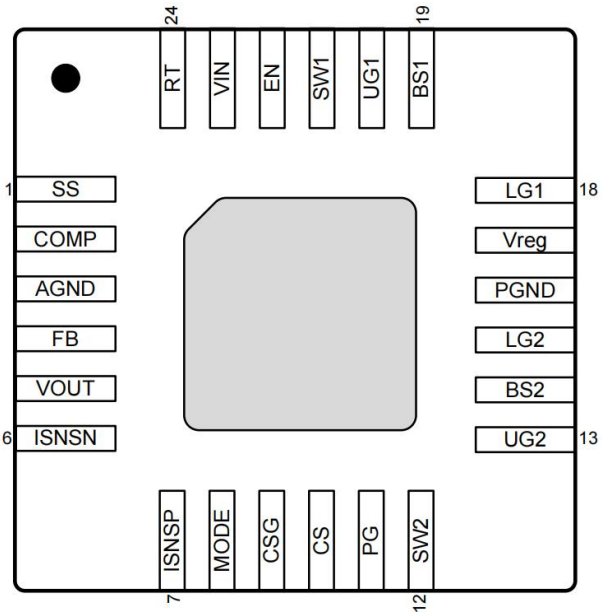
14.Place the Vreg bypass capacitor close to the controller IC, between the Vreg and PGND pins. A 2.2-μF ceramic capacitor is typically used.

15.The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connects to the exposed pad should be maximized to improve thermal performance.

16.Multi-layer PCB design is recommended.

Pin Description

TOP VIEW



(QFN4x4-24)

Pin No.	Pin Name	Pin Description
1	SS	Soft-start programming pin. A capacitor between the SS pin and AGND pin programs soft-start time.
2	COMP	Compensation Pin. This pin is used to compensate the regulation control loop. Connect a series RC network from COMP pin to GND.
3	AGND	Analog Ground Pin.
4	FB	Voltage Feedback Input Pin. Connecting FB and VOUT with a resistive voltage divider.
5	VOUT	VOUT sense input. Connect to the output capacitor.
6, 7	ISNSN, ISNSP	Output Current Sense Amplifier inputs. An optional current sense resistor connected between ISNSN and ISNSP can be located on the output side of the converter.
8	MODE	Connect this pin to AGND with 100kΩ resistor.
9	CSG	The negative or ground input to the PWM current sense amplifier. Connect directly to the low-side (ground) of the current sense resistor.
10	CS	The positive input to the PWM current sense amplifier.
11	PG	Power Good open drain output. PGOOD is pulled low when FB is outside a 0.8 V ±10% regulation window.
12, 21	SW2, SW1	The boost and the buck side switching nodes respectively.
13, 20	UG2, UG1	Output of the high-side gate drivers. Connect directly to the gates of the high-side MOSFETs.
14, 19	BS2, BS1	High Side Gate Drive Boost Input. A 100nF capacitor is recommended to connect from this pin to SW1, SW2. It can boost the gate drive to fully turn on the internal high side NMOS.
15, 18	LG2, LG1	Output of the low-side gate drivers. Connect directly to the gates of the low-side MOSFETs.

16	PGND	Power ground of the IC. The high current ground connection to the low-side gate drivers.
17	Vreg	Output of the VCC bias regulator. Connect 2.2μF to 4.7μF capacitor to ground.
22	EN	Enable Input Pin. This pin provides a digital control to turn the converter on or off.
23	VIN	Power Supply Input Pin.
24	RT	Switching frequency programming pin. An external resistor is connected to the RT pin and AGND to set the switching frequency.
Power Pad	-	Exposed Pad. Connecting to PCB Ground.

Order Information

Model	Package	T/R Qty.
TX9575-AFHR	QFN4x4-24L	5000PCS

*A: Output Voltage Adjustable

Absolute Maximum Ratings(1)

Input Supply Voltage V_{IN} ..... -0.3V ~ 42V
Enable Voltage V_{EN} ..... -0.3V ~ 42V
SW Voltage V_{SW1}, V_{SW2} .....-0.3V(-5V for < 10ns) ~ 42V (46V for < 5ns)
BS1 and UG1 Voltage V_{BS1}, V_{UG1} with respect to SW1..... -0.3 ~ (VSW + 6V)
BS2 and UG2 Voltage V_{BS2}, V_{UG2} with respect to SW2..... -0.3 ~ (VSW + 6V)
V_{OUT} , ISNSP, ISNSN Voltage..... -0.3V ~ 28V
All Other Pins Voltage ..... -0.3V ~ 6V
Maximum Junction Temperature ..... 150°C
Storage Temperature ..... -55°C ~ 150°C
Lead Temperature (Soldering 10 sec) .....260°C
ESD Classification (HBM) .....Class 2
Power Dissipation (P_D) @ TA = 25°C 1.92W

Recommended Operating Conditions (2)

Input Supply Voltage V_{IN} ..... 5V ~ 40V
Ambient Temperature T_A ..... -40°C ~ 85°C

Thermal Characteristics

QFN4x4-24(Exposed Pad), θ_{JA} ..... 52°C/W
QFN4x4-24(Exposed Pad), θ_{JC} ..... 7°C/W

Notes:

(1) Stresses exceed those ratings may damage the device.

(2) If out of its operation conditions, the device is not guaranteed to function.

Electrical Characteristics

V_{IN}=12V, T_A=25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage V_{IN}						
V_{IN} Input Supply Voltage			4.5		40	V
Quiescent Current (non-switching)	I_Q	V_{FB} = 1V		2		mA
Standby Supply Current (no loading)				6		mA
Regulator Voltage V_{reg}						
Regulation Voltage	V_{reg}			5.4		V
EA(Error Amplifier)						
Reference Voltage	V_{REF}	9V≦V_{IN}≦40V		808		mV
Error Amplifier GM	GM_{EA}			1.3		mS
COMP Sink/Source Current	I_{sink}/I_{source}	V_{FB}= V_{REF}±0.3V		250		uA
Frequency						
Switching Frequency	F_{SW}	RT=100KΩ		260		KHz
Current Limit						
Buck Current Limit Threshold	$V_{CS(BUCK)}$			76		mV
Boost Current Limit Threshold	$V_{CS(BOOST)}$			170		mV
Constant Current Loop						
Average Current Loop Regulation	V_{SNS}			50		mV
PG						
Trip Threshold for falling FB		Respect to V_{REF}		-10		%
Trip Threshold for rising FB		Respect to V_{REF}		10		%
EN/UVLO						
EN High-Level Input Voltage	V_{ENH}		1.8			V
EN Low-Level Input Voltage	V_{ENL}				0.4	V
Input UVLO Threshold		VIN Rising		4.2	4.5	V
Under Voltage Lockout Threshold Hysteresis				650		mV
SS						
Soft Start Pull Up Current	I_{SS}	V_{SS} = 0		6		uA
SS Clamp Voltage	$V_{SS(CLP)}$	SS Open		1.46		V
Thermal Shutdown						
Thermal Shutdown Threshold(3)				160		℃

Notes:

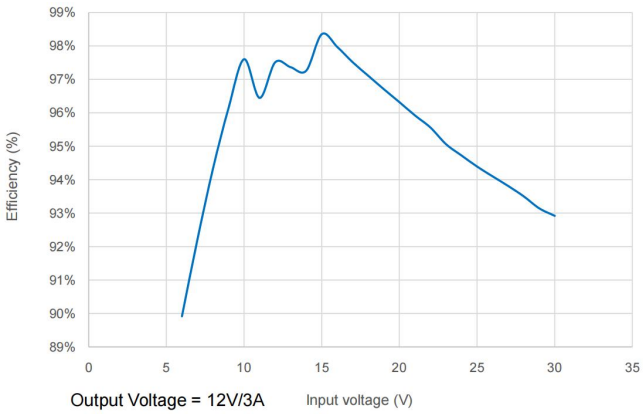
(3) Guaranteed by design.

Typical Performance Characteristics(1) (2)

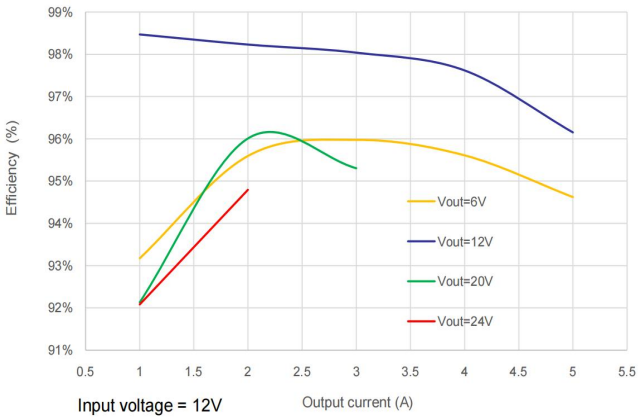
Note (1): Performance waveforms are tested on the evaluation board.

Note (2): At T_A = 25ºC, unless otherwise noted.

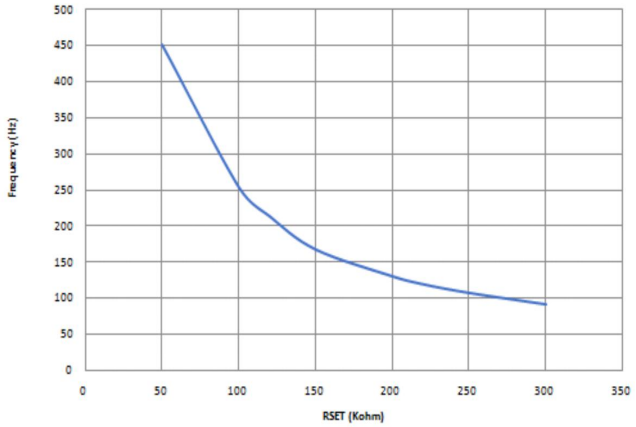
(1) Efficiency vs V_{IN}



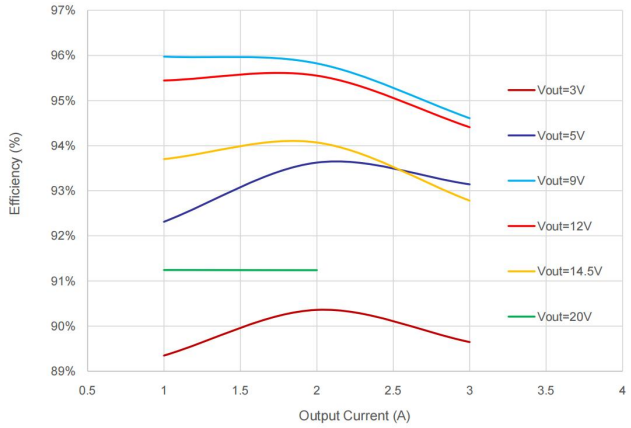
(2) Efficiency vs Load



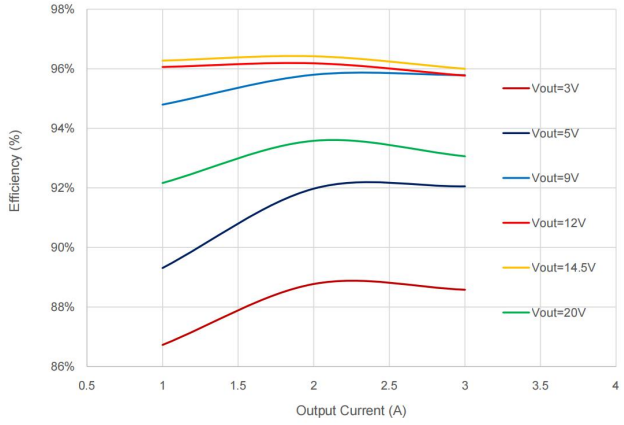
(3) Oscillator Frequency



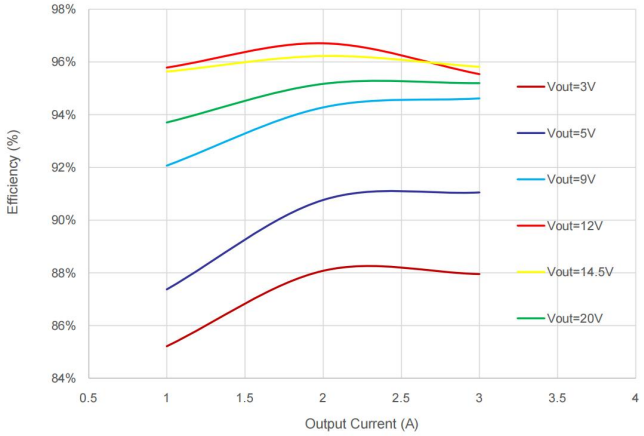
(4) Efficiency (Vin=9V)



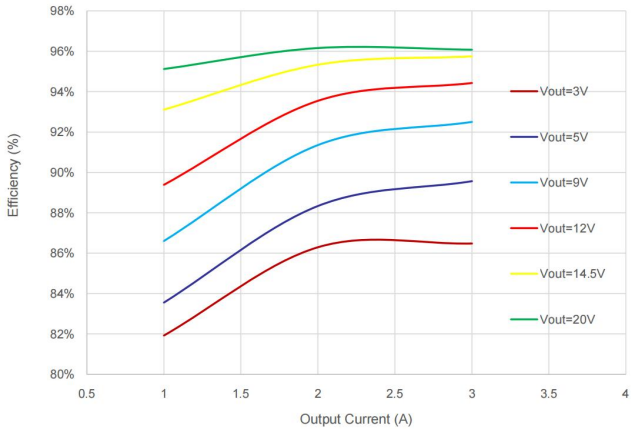
(5) Efficiency (Vin=12V)



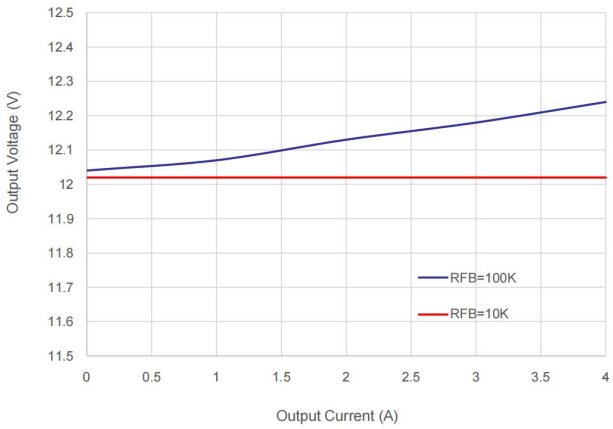
(6) Efficiency (Vin=14.5V)



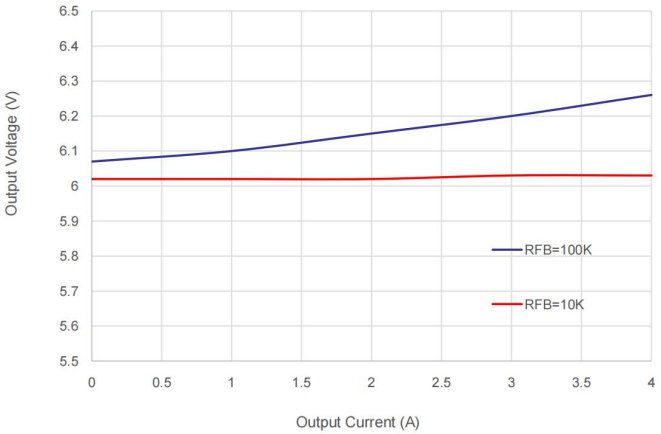
(7) Efficiency (Vin=20V)



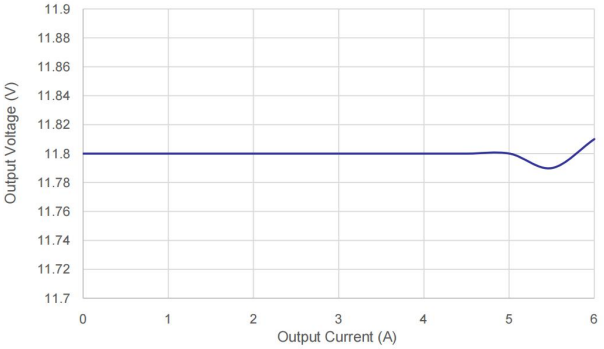
(8) Cable Compensate(V_{OUT}=12V)



(9) Cable Compensate(VOUT=6V)



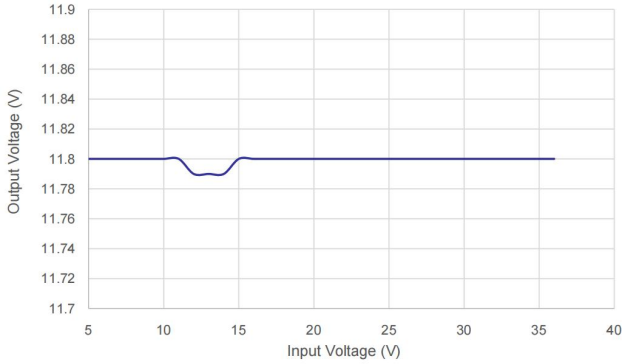
(10) Load Regulation



Test Condition :

VIN=12V, VOUT=12V, IOUT=0A~6A

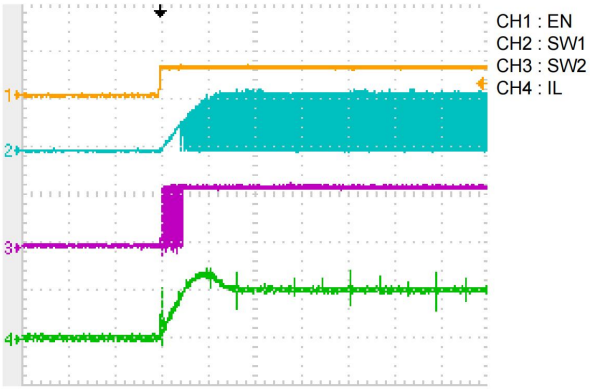
(11)Line Regulation



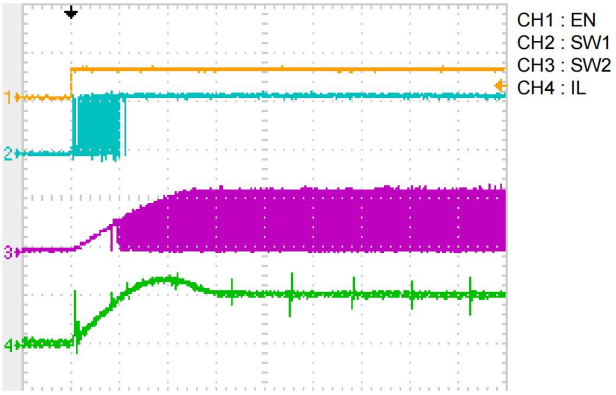
Test Condition :

VOUT=12V, VIN=5~36V, IOUT=1A

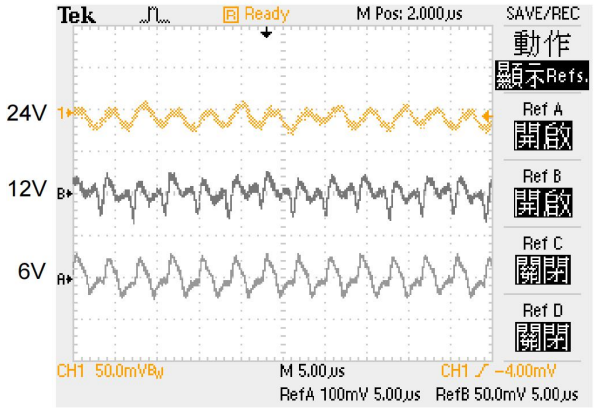
(12)Start-up(Buck Mode)



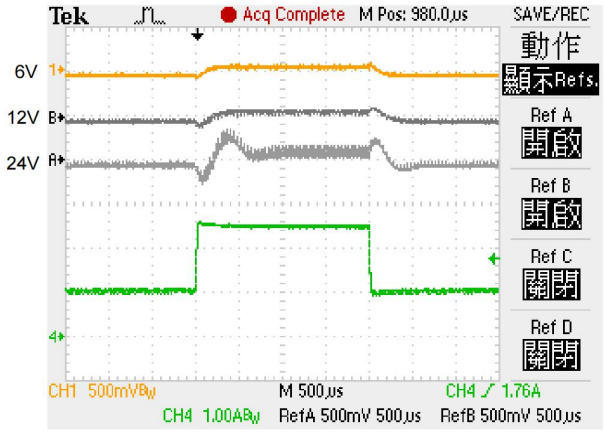
(13) Start-up(Boost Mode)



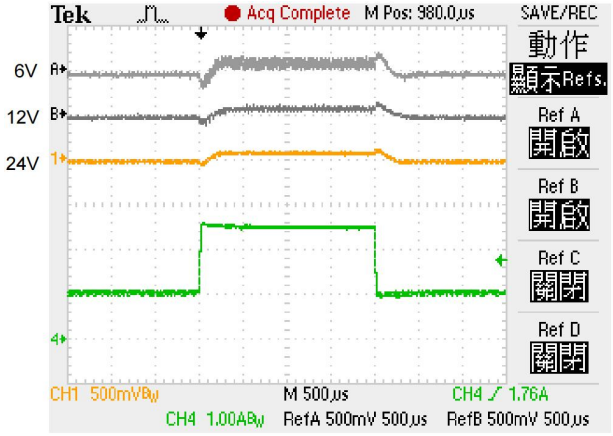
(14) Output Ripple (VIN:6V,12V,24V,VOUT:12V/2A)



(15) Load Transient (VIN=12V, VOUT=6V, 12V, 24V)

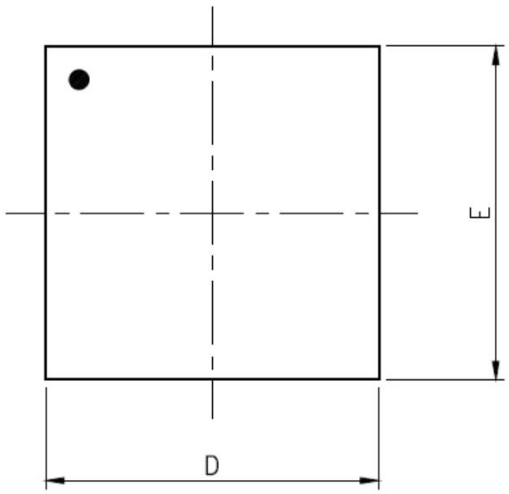


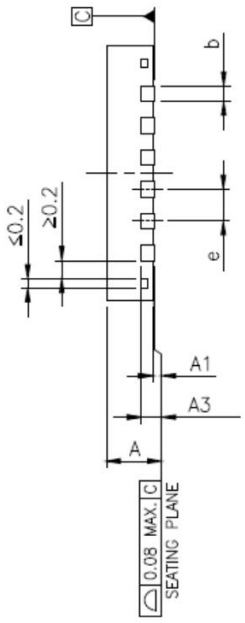
(16) Load Transient(VIN=6V, 12V, 24V VOUT=12V)

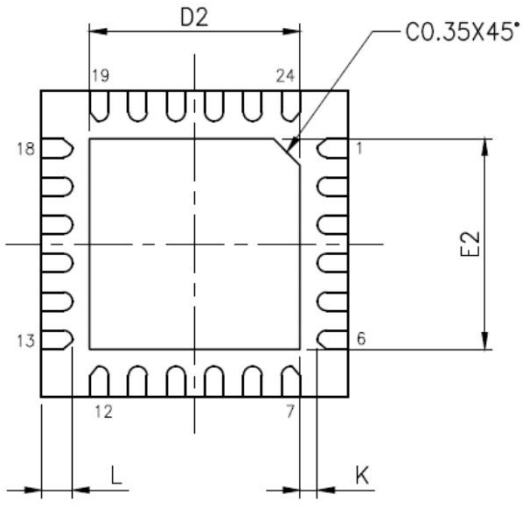


Package Description

QFN4X4-24L Outline Dimensions







UNIT:mm

SYMBOLS	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
K	0.20	---	---
D2	2.65	2.70	2.75
E2	2.65	2.70	2.75
L	0.35	0.40	0.45