TX9572

Features

- Wide Input Voltage from 4.5V to 40V
- Adjustable Switching Frequency
- High Efficiency
- High Duty-Cycle Up to 99%
- Programmable External Soft-Start
- CC/CV Control
- Auto Recovery after Fault
- Low Output Short Current
- Programmable Over Current Setting
- Over-Temperature Protection
- Thermal Enhanced TSSOP14,QFN4*4-16L Package
- ROHS Compliant

Applications

- Car Charger
- Rechargeable Portable Devices
- USB Power Delivery
- Automotive Industry

General Description

The TX9572 is a synchronous buck controller capable of regulating the output voltage below the input voltage. The TX9572 operates over a wide input voltage range of 4.5V to 40V to support a variety of applications.

The TX9572 employs voltage-mode control for superior load and line regulation. The switching frequency is programmed by an external resistor. This device also features a programmable soft-start function and offers protection features including cycle-by-cycle current limiting, input undervoltage lockout (UVLO) and thermal shutdown.

The TX9572 is available in a TSSOP14,QFN4*4-16L packages, provides a very compact system solution and good thermal conductance.

Typical Application

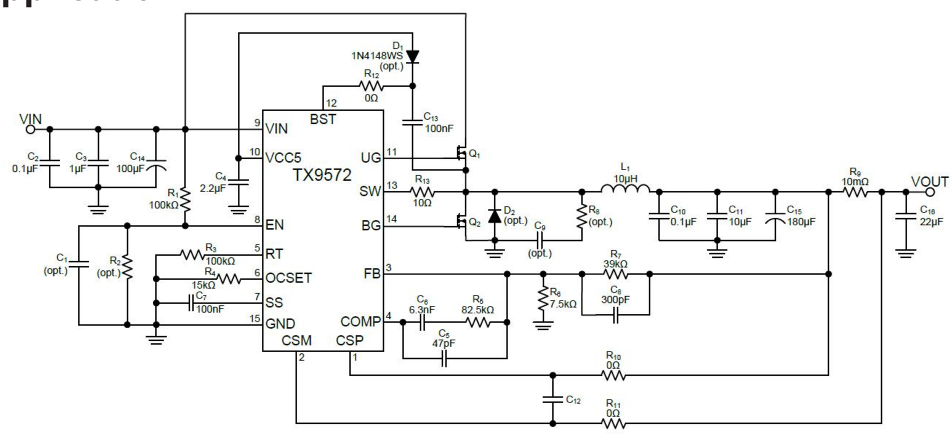


Figure 1 Simplified Application Circuit

System Block Diagram

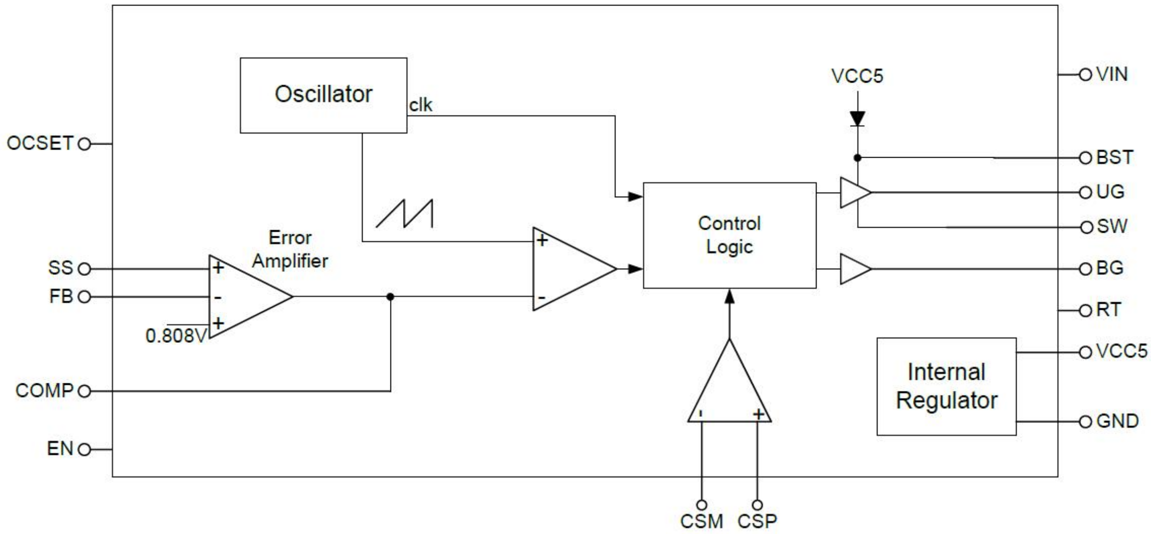


Figure 2 TX9572 Functional Block Diagram

Function Description

The TX9572 is a constant frequency synchronous step-down controller with integrated drivers for N-channel MOSFETs. It integrates a low-side driver and a high-side driver, eliminating the need for external drivers or floating bias supplies. The internal regulator supplies internal bias rails as well as the MOSFET gate drivers.

The PWM control scheme is based on voltage mode control. The inductor current is sensed through the low-side MOSFET. The sensed current is also monitored for cycle-by-cycle current limit.

In addition to the cycle-by-cycle current limiting, the TX9572 also provides output current regulation that can be configured for output current limiting and short circuit protection. This is useful for battery charging or other applications where a constant current behavior may be required.

The soft-start time of TX9572 is programmed by a capacitor connected to the SS pin to minimize the inrush current and overshoot during startup.

Control Loop

During normal operation, the output voltage is sensed at FB pin through a resistive voltage divider and amplified through the error amplifier. The voltage of error amplifier output pin COMP is compared to the internal sawtooth reference to controls the RS latch. At each cycle, the high-side MOSFET would be turned on when the oscillator sets the RS latch and would be turned off when current comparator resets the RS latch. When the load current increases, the FB pin voltage drops below reference voltage (V_{REF}) 0.808V, it causes the COMP voltage increase until average inductor current arrive at new load current.

Input Under Voltage Lockout

When the TX9572 power on, the internal circuits are held inactive until VIN exceeds the input UVLO threshold voltage. And the regulator will be disabled when VIN below the input UVLO threshold voltage.

Internal Regulator

In TX9572, the internal regulator provides a regulated 5.25V supply with adequate VIN voltage to the gate drivers. For low VIN operation, ensure that the VCC5 voltage is sufficient to fully enhance MOSFETs. A 2.2uF to 4.7uF capacitor to GND is recommended to supply the regulator load transients.

Soft Start

The TX9572 soft-start time is programmed using a soft-start capacitor from the SS pin to GND. When the controller is enabled, an internal 6uA current source charges the soft-start capacitor. When the SS pin voltage is below the FB reference voltage (V_{REF}) 0.808V, the SS pin controls the regulated FB voltage. Once SS exceeds V_{REF}, the soft-start interval is complete and the error amplifier is reference to V_{REF}. The soft-start time is roughly given by below equation:

$$tss = \frac{C7X0.808}{6u}(\text{sec})$$

Over Current Protection

The TX9572 provides cycle-by-cycle current limit to against over current and short circuit conditions. OCSET pin is connected to a resistor (R_{OCSET}) to set current limit value. The sensed valley voltage across the low-side MOSFET is limit by below equation:

$$V_{LG\_MOS} = 10u \times R_{OCSET}\ (V)$$

The valley current limit in the low-side MOSFET can be calculated by the equation:

$$I_{LG_{MOS}} = \frac{V_{LG\_MOS}}{R_{ON(LGMOS)}}\ (A)$$

Output Current Limit

The TX9572 provides output current limiting capability. A current sense amplifier with inputs at the CSP and CSM pins monitors the voltage across the sense resistor (R_{SNS}). The current limiting feature can be used in applications requiring a regulated current from the load. The target constant current is given by below equation:

$$I_{OUT(AVG)} = \frac{50\text{m}}{R_{SNS}}(\text{A})$$

The current loop can be disable be shorting the CSP and CSM pins to VOUT.

Over Temperature Protection

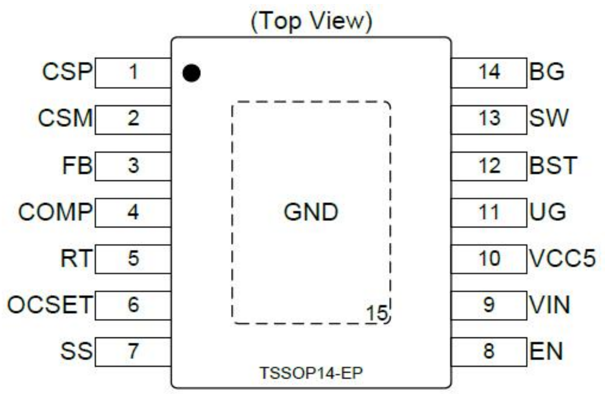
The TX9572 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown.

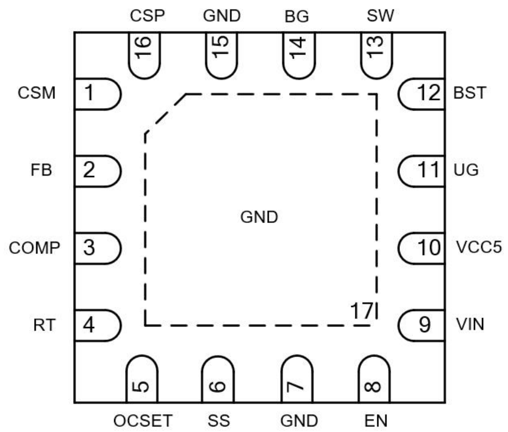
Switching Frequency

The TX9572 switching frequency is programmed used a resistor (R_{RT}) from RT pin to GND. The switching frequency (f_{SW}) is roughly given by below equation:

$$\text{fsw} = \frac{25e^6}{R_{RT(\Omega)}}(\text{khz})$$

Pin Configuration





Pin Description

Pin NO.		Pin Name	Pin Description
TSSOP14L	QFN4×4-16L		
1	16	CSP	Positive input pin for output load current sensing.
2	1	CSM	Negative input pin for output load current sensing.
3	2	FB	Voltage Feedback Input Pin. Connecting FB and VOUT with a resistive voltage divider. This IC senses feedback voltage via FB and regulate it at 0.808V.
4	3	COMP	Compensation Pin. This pin is used to compensate the regulation control loop. Connect a series RC network from COMP pin to FB pin.
5	4	RT	Switching frequency programming pin. An external resistor is connected to the RT pin and GND to set the switching frequency
6	5	OCSET	Valley current limit programming pin. An external resistor is connected to the OCSET pin and GND to set the valley current limit.
7	6	SS	Soft-start programming pin. A capacitor between the SS pin and GND programs soft-start time.
8	8	EN	Enable Input Pin. This pin provides a digital control to turn the controller on/off.
9	9	VIN	Power Supply Input Pin. Drive 4.75V to 40V voltage to this pin to power on this chip. Connecting a 10uF ceramic bypass capacitor between VIN and GND to eliminate noise.
10	10	VCC5	BG Driver Bias Supply. Decouple with a 2.2uF capacitor
11	11	UG	Output of the high-side gate driver. Connect to the gate of the high-side MOSFET
12	12	BST	High Side Gate Drive Boost Input. A 100nF capacitor is recommended to connect from this pin to SW. It can boost the gate drive to fully turn on the external high-side MOSFET.
13	13	SW	Power Switching Output. It is the output pin that internal high side NMOS switching to supply power
14	14	BG	Output of the low-side gate driver. Connect to the gate of the low-side MOSFET.
15	15,17	GND	Exposed Pad. Ground Pin.

Order Information

Part Number	Package	Shipment
TX9572TP14R	TSSOP14	Tape & Reel / 4000
TX9572FTR	QFN4*4-16L	Tape & Reel / 3000

Absolute Maximum Ratings(1)

Input Supply Voltage V_{IN} .... -0.3V ~ 42V

EN Voltage V_{EN} .... -0.3V ~ 42V

CSP, CSM Voltage V_{CSP}, V_{CSM} .... -0.3V ~ 24V

SW Voltage V_{SW} ....-0.3V(-5V for < 10ns) ~ 42V (46V for < 5ns)

Boost Voltage V_{BST} .... -0.3 ~ (V_{SW} + 6V)

UG Voltage V_{UG} .... V_{SW} ~ (V_{SW} + 6V)

All Other Pins Voltage .... -0.3V ~ 6V

Maximum Junction Temperature .... 150°C

Storage Temperature .... -55°C ~ 150°C

Lead Temperature (Soldering 10sec) ....260°C

ESD Classification(HBM) ....Class 2

Power Dissipation (P_D)TSSOP-14 @T_A = 25°C ...2.5W

Power Dissipation (P_D)QFN4*4-16@T_A = 25°C ... 2.63W

Recommended Operating Conditions(2)

Input Supply Voltage V_{IN} .... 5V ~ 40V

Ambient Temperature T_A ....-40°C~85°C

Thermal Characteristics

TSSOP14(Exposed Pad),θ_{JA} .... 40°C/W

QFN4*4-16(Exposed Pad), θ_{JA}.........................38°C/W

TSSOP14(Exposed Pad),θ_{JC} .... 7.5°C/W

QFN4*4-16(Exposed Pad),θ_{JC} .... 4.5°C/W

Notes(1): Stresses exceed those ratings may damage the device.
Notes(2): If out of its operation conditions, the device is not guaranteed to function.

Electrical Characteristics

V_{IN}=12V, T_A=25℃, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN} Input Supply Voltage	---	---	4.5	---	40	V
Quiescent Current (non-switching)	I_Q	V_{FB}=0.85V	---	1.5	2	mA
Standby Supply Current (no loading)	---	---	---	---	20	mA
Regulation Voltage	V_{CC5}	---	4.5	5.25	---	V
Feedback Reference Voltage	V_{FB}	4.5V≦V_{IN}≦40V	792	808	824	mV
Error Amplifier Transconductance(3)	G_{EA}	Δ_{ICOMP} = ±10μA	---	850	---	μA/V
Switching frequency	F_{SW}	RT=100kΩ	200	250	300	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V	97	98	99	%
Minimum On Time	T_{ON}	---	---	250	---	ns
Over Current Sensing Threshold Voltage	V_{SNS}	V_{SNS}=V_{CSP}-V_{CSM}, V_{CSM}=5V	---	50	---	mV
Input UVLO Threshold	---	VIN Rising	---	4.2	4.4	V
Input UVLO Threshold Hysteresis	---	---	---	600	---	mV
Soft-Start Pull Up Current	I_{SS}	V_{SS}=0	---	6	---	uA
SS Clamp Voltage	$V_{SS(CLP)}$	SS Open	---	1.46	---	V
Thermal Shutdown Threshold(3)	---	---	---	160	---	℃
Gate Driver Sink Impedance(3)	R_{Sink}	---	---	0.9	---	Ω
Gate Driver Source Impedance(3)	R_{Source}	---	----	3.3	---	Ω
EN High-Level Input Voltage	V_{ENL}	---	2.0	---	---	V
EN Low-Level Input Voltage	V_{ENL}	---	---	---	0.4	V

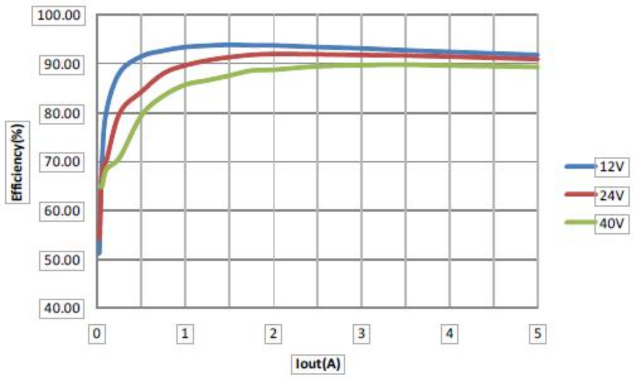
Note:(3) Guaranteed by design.

Typical Performance Characteristics

Freq=250KHZ, L1 = 10uH,TA = +25℃, unless otherwise noted.

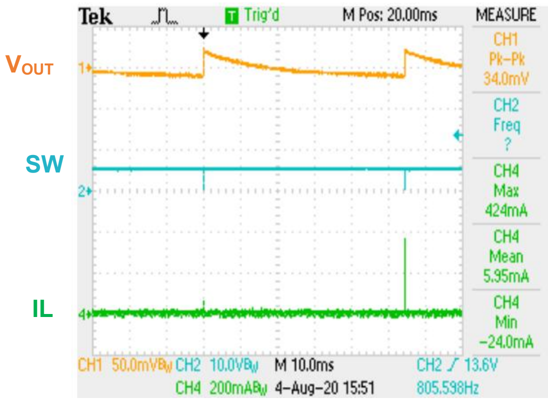
Efficiency Test

Vout=5V,Freq=250KHZ



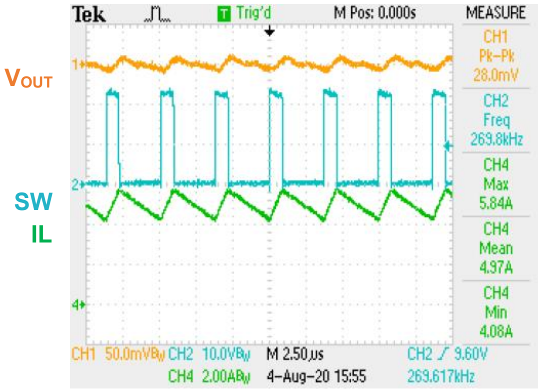
Steady State

Vin=24V,Vout=5V,Iout=0A



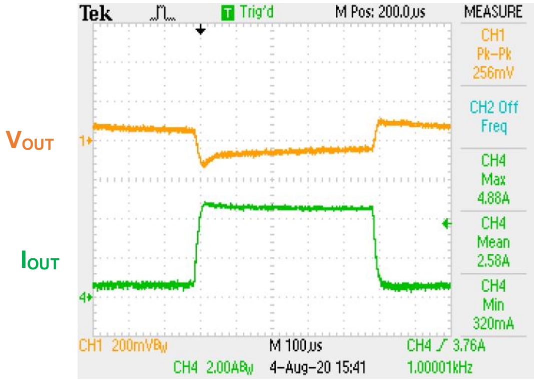
Steady State

Vin=24V,Vout=5V,Iout=5A



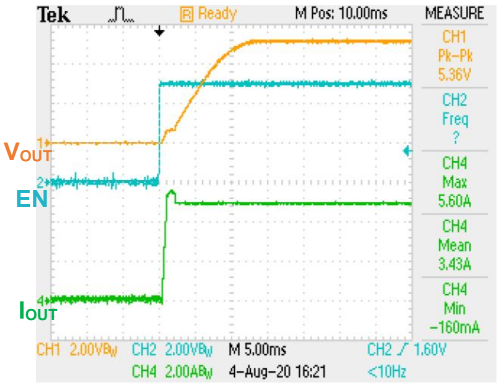
Dynamic loading

Vin=24V,Vout=5V,Iout=0.5 to 4.5A



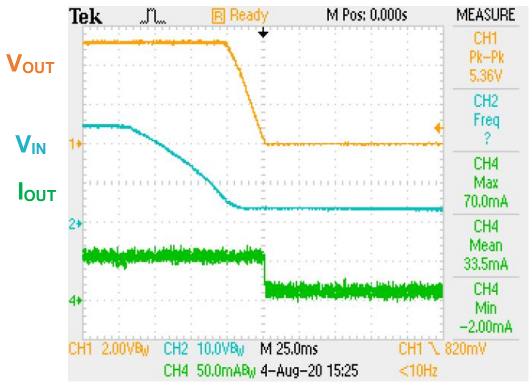
Power On

Vin=24V,Vout=5V,Iout=5A



Shut Down

Vin=24V,Vout=5V,Iout=0.05A



Applications Information

Output Voltage Setting

The output voltage V_{OUT} is set using a resistive divider from the output to FB. The FB pin regulated voltage is 0.808V. Thus the output voltage is:

$$V_{OUT} = 0.808 \times \left(1 + \frac{R7}{R6}\right) V$$

Place resistors R_7 and R_6 close to FB pin to prevent stray pickup.

Input Capacitor Selection

The use of the input capacitor is controlling the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 times to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IIN(RMS)} = I_{OUT} \times \sqrt{D * (1 - D)}$$

Where D is the duty cycle and the value is V_{OUT} / V_{IN}. A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When the using tantalum or electrolytic capacitors, a 0.1uF ceramic capacitor should be placed as close to the IC as possible.

Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. Low ESR capacitors are preferred. Ceramic, tantalum or low ESR electrolytic capacitors can be used, depends on the output ripple requirement. Add a 100uF or 470uF low ESR electrolytic capacitor when operated in high input voltage range (VIN > 20V). It can improve the device's stability. The output ripple voltage ΔV_{OUT} is described as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)\left(R_{ESR} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}}\right)$$

Where f_{SW} is the switching frequency, L is the inductance value, V_{IN} is the input voltage, V_{OUT} is the output voltage, R_{ESR} is the equivalent series resistance value of the output capacitor, and the C_{OUT} is the output capacitor. When using the ceramic capacitors, the R_{ESR} can be ignored and the output ripple voltage ΔV_{OUT} is shown as:

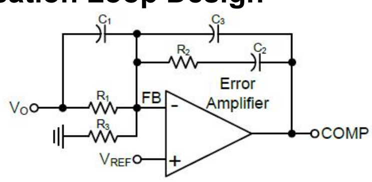
$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \cdot {f_{sw}}^2 \cdot L \cdot C_{OUT}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

When using tantalum or electrolytic capacitors, typically 90% of the output voltage ripple is contributed by the ESR of output capacitors. the output ripple voltage ΔV_{OUT} can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{sw} \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. TX9572 can be optimized for a wide range of capacitance and ESR values.

Compensation Loop Design



The following guidelines will help users to design the compensation network.

(1) Select the desired zero crossover frequency f_C. f_C is usually 1/4 ~ 1/10 switch frequency (f_{SW})

(2) Choose zero frequency $\frac{1}{2\Pi R1C1}$ = fc

(3) Choose $\frac{R2}{R1} = \frac{(2\Pi fc)^2(0.04V_{IN}+0.4)LC_O}{V_{IN}}$

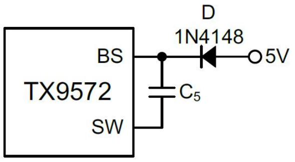
(4) Choose $\frac{1}{R2C2} = \frac{1}{10}\sqrt{\frac{1}{LC_O}}$

(5) Choose $R_2C_3 = R_{ESR}\cdot C_O$ to cancel lead effect of ESR.

Where L is the inductor value, C_O is the output capacitance and R_{ESR} is ESR of the output capacitor.

External Boost Diode Selection

For duty cycle larger than 65% applications, it is recommended that an external boost diode be added. This helps improve the efficiency. The boost diode can be a low cost one such as1N4148.



PCB Layout Guideline

The device's performance and stability is dramatically affected by PCB layout. It is recommended to follow these general guidelines show bellow:

1.Keep the traces of the main current paths as short and wide as possible to minimize parasitic inductance and resistance.

2.Place V_{IN} bypass capacitor (CIN) close to the device pins (VIN and GND). The loop area formed by CIN and VIN/GND pins must be minimized.

3.Minimize the switching loop area formed by VIN, SW and the power MOSFETs of UG and BG.

4.Use a combination of bulk capacitors and smaller ceramic capacitors with low series impedance for the input and output capacitors. Place the smaller capacitors closer to the IC.

5.Place feedback resistors close to the FB pin. Connect feedback network behind the output capacitors.

6.Place compensation components close to the COMP pin.

7.Place the BST bootstrap capacitor close to the IC and connect directly to the BST to SW pins

8.Keep the sensitive signal (FB, COMP, CSP, CSM, RT, OCSET and SS) away from the switching signal (BST, SW, UG, BG).

9.Use Kelvin connections to sense resistor for the current sense signals CSP and CSM.

10.Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacities.

11.Place the VCC5 bypass capacitor close to the controller IC, between the VCC5 and GND pins.

12.The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connects to the exposed pad should be maximized to improve thermal performance.

13.Multi-layer PCB design is recommended.

Typical Application

Fix 5V Output Voltage

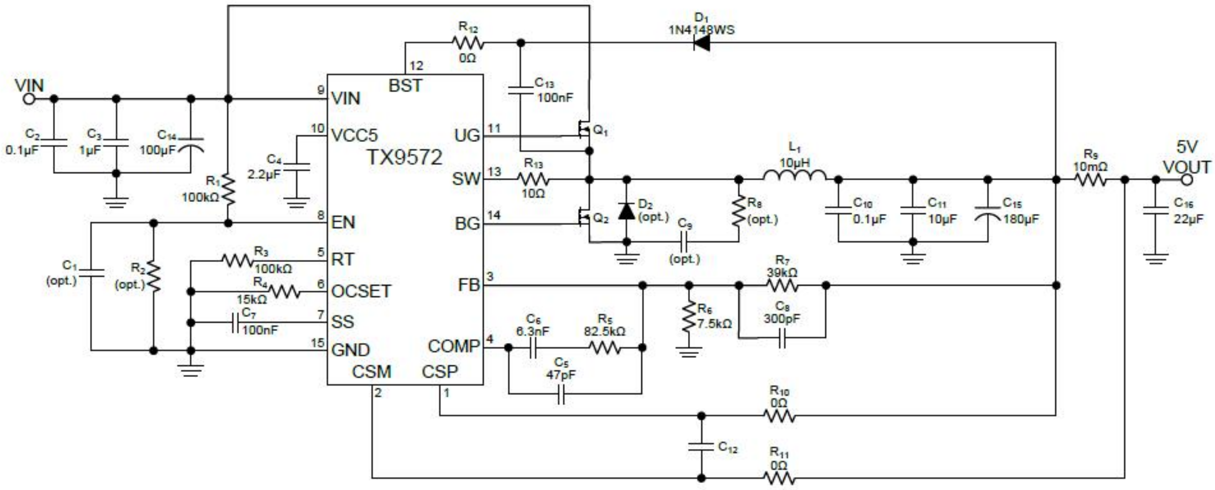


Figure 3 For 5V Output Voltage Application Circuit

Input Voltage < 5.5V

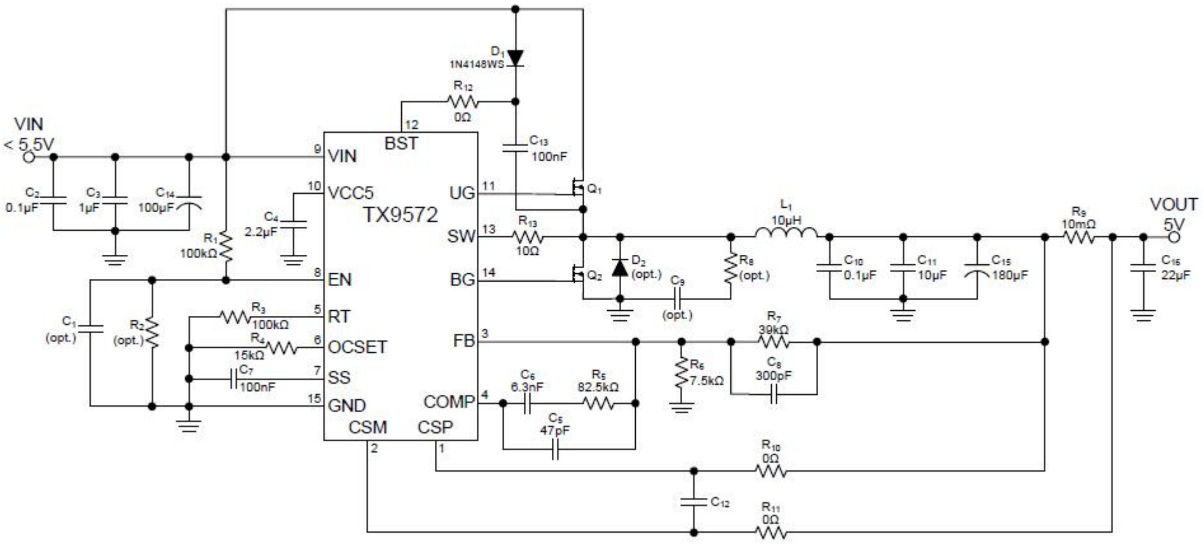
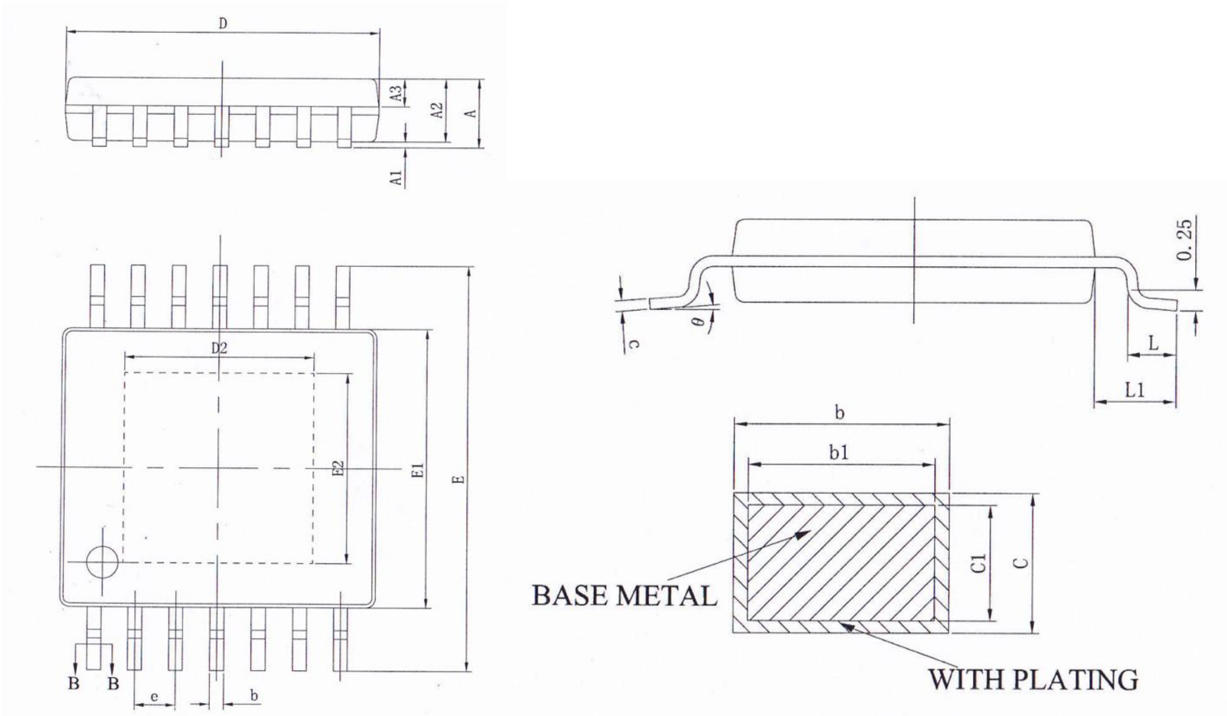


Figure 4 For VIN < 5.5V Application Circuit

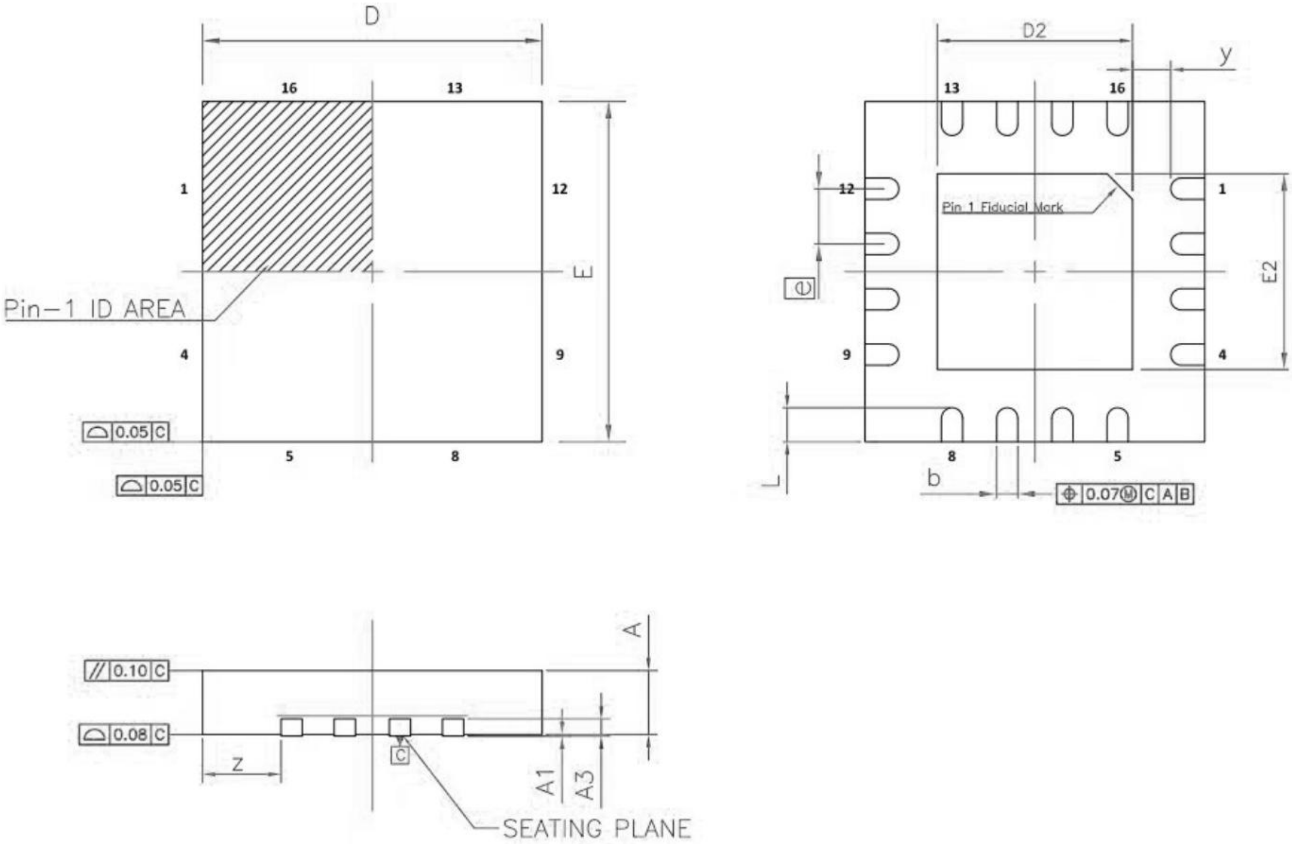
TSSOP-14 PACKAGE INFORMATION



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

Size(mm) / L/F Size (mil)	D2	E2
79*79	1.80REF	1.80REF
124*122	2.95REF	2.90REF

QFN4*4-16L PACKAGE INFORMATION



符号	尺寸（毫米）		
	最小值	典型值	最大值
D	3.95	4.00	4.05
E	3.95	4.00	4.05
D2	2.20	2.30	2.40
E2	2.20	2.30	2.40
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
e	0.650 BSC		
K	---	---	---
L	0.35	0.40	0.45
Y	0.450 REF		
Z	0.925 REF		